EE 471: Transport Phenomena in Solid State Devices

HW5

Due: 3/27/18

Please show all working (including equations you use to calculate your answers).

All numerical answers should include units

Calculate numerical answers to 3 sig. figs.

1. A silicon MOS capacitor is built by placing an N^+ poly gate over a P-type substrate with $N_A = 5 \times 10^{16}\ cm^{-3}$ and a gate oxide thickness of $15\ nm$. Calculate:

    a) Gate oxide capacitance (per unit area) *(2 points)*
    b) Flatband voltage *(3 points)*
    c) Threshold voltage *(4 points)*
    d) Accumulation charge (per unit area) at $V_g = -2V$ and $V_g = +2V$ *(4 points)*
    e) Depletion charge (per unit area) at $V_g = -2V$ and $V_g = +2V$ *(5 points)*
    f) Inversion charge (per unit area) at $V_g = -2V$ and $V_g = +2V$ *(4 points)*
    g) What is the voltage across the oxide at $V_g = +2V$ *(3 points)*
    h) Suppose the doping density in the N^+ poly gate is $2 \times 10^{19}\ cm^{-3}$. Assuming the V_{ox} value you calculate in part (g), determine the width of the small depletion region that forms in the poly gate at the poly-oxide interface. How does this (quantitatively) change the effective oxide thickness? (4 points extra credit)