EE 471: Transport Phenomena in Solid State Devices

HW6

Due: 4/3/18

Please show all working (including equations you use to calculate your answers).

All numerical answers should include units

Calculate numerical answers to 3 sig. figs.

1. An ideal NMOS transistor has the following parameters:
   - $W = 6\mu m,\ L = 0.13\mu m$
   - $T_{oxe} = 5\ nm$
   - $W_{dmax} = 60\ nm$
   - $V_t = 0.3\ V$
   - $\mu_{ns} = 350\ cm^2/V.s$

   Determine:

   a) Gate capacitance per unit area C_{oxe} (3 points)
   b) Transistor β (3 points)
   c) Bulk charge factor m (3 points)
   d) V_{dsat} and I_{dsat} at $V_{gs} = 1.0V$ and $1.5V$ (10 points)
   e) Sketch I_{ds} *vs.* V_{ds} curves for $0 < V_{ds} < 2.0V$ and $V_{gs} = 1.0\ and\ 1.5V$ (6 points)

2. Repeat problem #1 parts (d) and (e), this time taking velocity saturation into account, given $v_{sat} = 9 \times 10^6\ cm/s$. Sketch the IV curves <u>on the same axes</u> you used in Q1, so that you can compare the results (15 points)

3. An NMOS transistor has $\beta = 2\ mA/V^2$, $m = 1.2$ and a threshold voltage of 0.5V.

   (a) What is the g_m of this transistor at $V_{gs} = 2.0V$? (2 points)
   (b) If this transistor was used in a simple common source amplifier with an effective load resistance of $10\ k\Omega$, what would you expect the gain of the amplifier to be at this bias, assuming ideal (Shockley model) behavior ? (3 pts)
   (c) When the circuit is built, however, the gain is measured at -15. Estimate the channel length modulation parameter λ. (3 points extra credit)