EE 471: Transport Phenomena in Solid State Devices

HW7

Due: 4/17/18

For this homework, you will download a free PC version of the industry standard SPICE circuit simulator called *LTspice*, provided by Linear Technologies – an analog IC design company. Using this simulator you will describe the circuit connectivity of a CMOS 2-input NAND gate and then perform a transient analysis of the NAND gate driving a capacitive load.

Part I: Downloading and Installing LTspice

Go to: http://www.linear.com/designtools/software

Click on *Download LTspice*. A pop-up window asks you if you want to receive software updates. Just click *No thanks* to download the software.

Once the installation program *LTspice.exe* has been downloaded, run the installation program. Follow the installation instructions, accept the terms of the license and install the software in the default location *C:\Program Files\LTC\LTspice*.

Create a working folder (somewhere in your user space) called SPICE (or any other name you prefer). We will use this folder to build SPICE simulation files. Open the folder, then right-click and select **New/Text Document** to create an empty file. Then change the name of that file from *New Text Document.txt* to *NAND.cir* Ignore the Windows warning about changing filename extensions.

Use the *SPICE 180nm CMOS models* link on the resources page on the course website to download the CMOS transistor model file. When you click on this link, the file will appear as text on your browser window. Use the **File/Save as** command in your browser pull-down menu to store this file in your working SPICE folder.

Part II: Modeling a CMOS NAND gate

A circuit schematic of the CMOS NAND gate we will be simulating is shown in Figure 1. It consists of two NMOS transistors and two PMOS transistors. There are 6 nodes in the circuit: inputs A and B, the output Y, power supplies VDD and GND and one internal node X. Width and lengths of each transistor are shown in microns. We will simulate this circuit assuming a 180nm CMOS process. The length of each transistor is set to the minimum size for this technology: 0.18 microns. The width of each transistor is set to approximately twice the minimum width: 0.8 microns. A 100fF capacitor is placed on the output as a load device. This simulates the capacitive load of other gates which may be driven by the output of this gate.

A SPICE netlist description of this circuit is shown in Figure 2. The *include* command loads the MOS transistor model file for the process we will be simulating. The models for the NMOS and CMOS devices referred to in the netlist are found in this file.

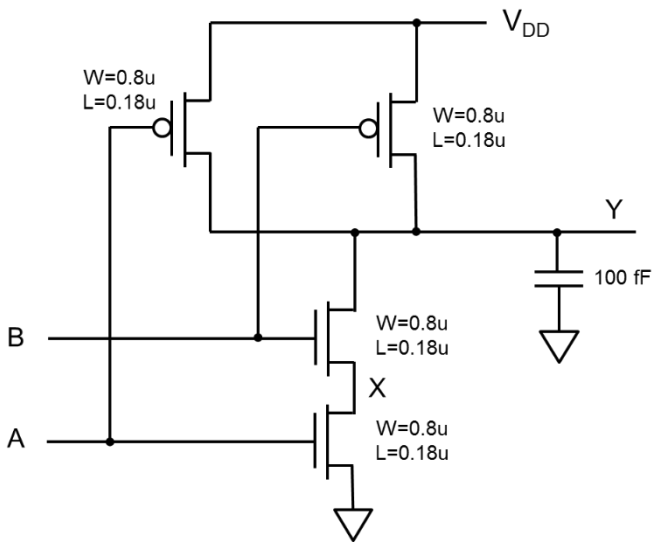

Fig. 1 Schematic of 2-input CMOS NAND gate

```
* Circuit netlist of NAND2 gate

.include "Mosis_tsmc_180nm.model"

MN1 X A GND GND NMOS L=0.18um W=0.8um
MN2 Y B X GND NMOS L=0.18um W=0.8um
MP1 Y A VDD VDD PMOS L=0.18um W=0.8um
MP2 Y B VDD VDD PMOS L=0.18um W=0.8um
Cout Y GND 100fF
```

Fig. 2 SPICE netlist of CMOS NAND gate

Run the LTspice simulator by going to the *Start Menu/All Programs* and double-clicking on the **LTspice** icon. Using the pull-down menu command File/Open, open the file *NAND.cir* in your working SPICE folder. At this stage, this is an empty file. Type or cut-and-paste the code form Fig. 2 into the text window.

In order to simulate the circuit, we need to apply a power supply voltage and some input waveforms. Append the SPICE commands shown in Fig. 3 to the code you already have in the *LTspice* text window. The first line sets the power supply (VDD) to be 3.3V by inserting a 3.3V voltage source between GND and VDD. The next two lines set up repeating pulse waveforms to drive the inputs A and B. The last line tells the simulator to perform a transient analysis for 100ns with a maximum time-step of 0.1ns.

```
Vvdd  VDD GND 3.3
VinA  A GND dc 0 pulse  0 3.3  0ns 0.1ns 0.1ns 25ns 50ns
VinB  B GND dc 0 pulse  0 3.3  12ns 0.1ns 0.1ns 25ns 50ns

.tran .1ns 100ns
```

Fig. 3 SPICE to set up and drive simulation

Run a simulation by selecting the  button. A blank waveform window will appear. Place your cursor in the waveform window, right-click and select **Add Plot Pane**. A second blank plot pane appears. Repeat this action to generate a third blank plot pane. Now right click in one of the panes and select **Add Trace**. This will produce a list of all the voltage and currents that are available to be plotted. Select **V(a)** and click **OK.** The input waveform of input A will now appear in this window. In similar fashion, select **V(b)** to appear in the second window and **V(y)** to appear in the third. These waveforms should show the correct operation of the two-input NAND gate. You can adjust the size of the sub-windows to suit your taste. Your simulation window should now appear similar to that shown in Figure 4. Note that the rise and fall times of the Y output is limited by the load capacitance that we have placed on this signal.

Use the pull down menus to select **Plot Settings/Save Plot Settings**. This will save your plot settings in a file named *NAND.plt* so that when you come back to simulate this circuit again, you won't have to set up the windows and traces again.

Part III: Evaluating gate delay vs. load capacitance

Determine the rising and falling propagation gate delay of this two input CMOS NAND gate as a function of load capacitance. Rising and falling propagation delays (t_{pdr} and t_{pdf}) are defined to be the delays from the time that the input signal crosses the VDD/2 voltage to the time that the output voltage crosses the VDD/2 voltage as shown in Fig. 5.

You can add two cursors to your plots to simplify the process of measuring delays. If you right click on the name of a trace (e.g. V[a]) immediately above its waveform), an *Expression Editor* window pops-up. Use the pull-down *Attached Curso*r menu to select **1st**, and then click **OK**. A dashed cursor will appear on the plot and another small pop-up window shows the position of the attached cursor. If you place the mouse over the attached cursor, the mouse cursor changes from a cross to the number '1'. If you now hold the left mouse button down you can move this cursor to any desired position on the waveform. If you do the same operations on another waveform and select *attached cursor* **2**, a second cursor will appear on this waveform and its position will also be shown on the pop-up. The pop-up window also tells you the time difference between the positions of the two cursors. You can use these do accurately measure the time delay between two events in your simulation. For more information on these attached cursors, go to *Waveform Viewer/Attached Cursors* in the *Help/Help Topics* pull-down menu.

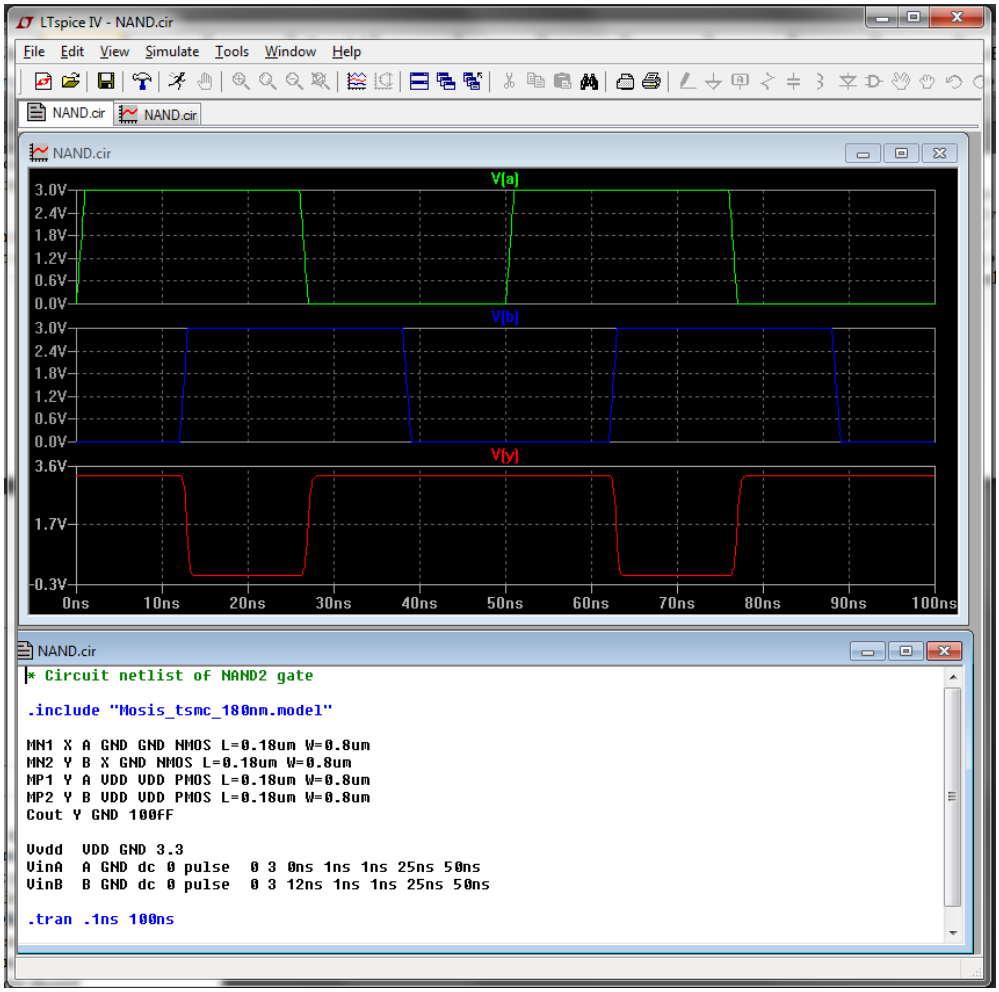

Fig. 4 *LTspice* window showing simulation results

Manually plot the rising and falling propagation delay vs. load capacitance for a range of load capacitance of 0 – 2 pf.

Write a brief report showing simulation waveforms at a few different values of load capacitance and your plot of rising and falling delay vs. load capacitance.

Note, when you are capturing screen shots for your report, you can make your plots more readable (and use less blank ink) by changing plot and background colors using the ***Tools/Color Preferences*** *pull-down menu and the thickness of the plot lines using the* ***Tools/Control Panel/Waveforms*** *pull-down.*

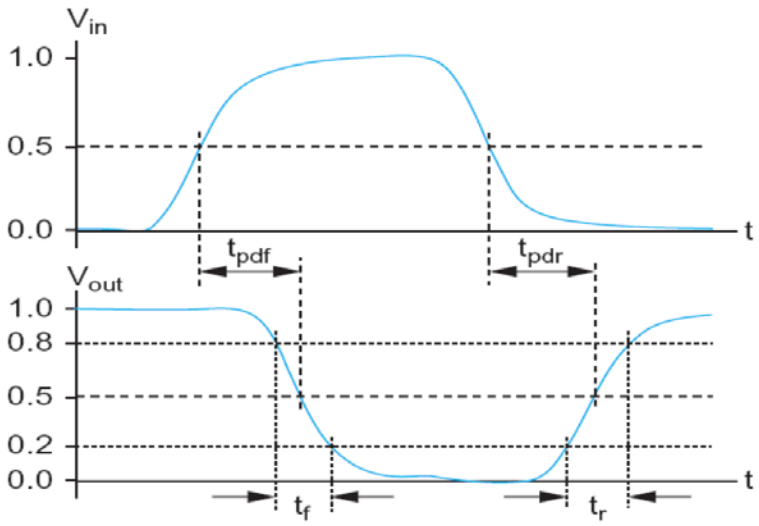

Fig. 5 Definition of Propagation delays