EE 471: Transport Phenomena in Solid State Devices

HW8

Due: 4/27/18

Please show all working (including equations you use to calculate your answers).

All numerical answers should include units

Calculate numerical answers to 3 sig. figs.

1. (a) Sketch a transistor-level schematic for a single-stage compound CMOS logic gate for the following function: (5 points)

$$Y = \overline{E.(C + A.B.D)}$$

(b) Draw a stick diagram to show the topology of a possible layout (10 points)

(c) Estimate the area of the gate (in units of λ^2) (5 points)

2. (a) Draw the schematic of a CMOS compound gate that implements $Y = \overline{B.C.(A + D)}$ (pick a topology that has the drain of the "*B"* NMOS transistor connected directly to the output "*Y" and the source of the "C" NMOS transistor connected directly to GND*). Size the transistor widths chosen to achieve effective rise and fall resistances equal to a unit inverter. (5 points)

b) Redraw your schematic and annotate with the effective resistance of each transistor and the effective capacitance of each node, assuming that every source or drain has a fully contacted diffusion (except for like-transistors in series which use a shared diffusion). Assume that the resistance and capacitance of a unit size NMOS transistor are R and C respectively. (6 points)

c) Compute the worst case rising and falling propagation delays of your gate driving **three** similar gates (via input A) using the Elmore delay model. Show your working. (14 points)