EE 471: Transport Phenomena in Solid State Devices

HW9

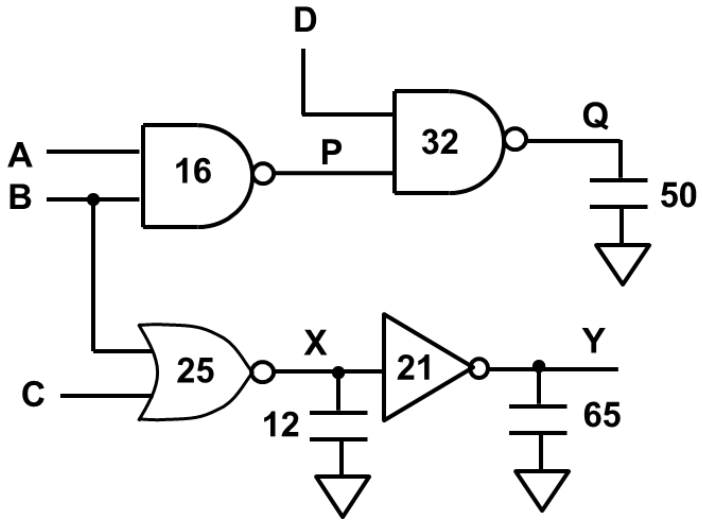
Due: 5/3/18

Please show all working (including equations you use to calculate your answers).

All numerical answers should include units

Calculate numerical answers to 3 sig. figs.

Consider the circuit below in which gate sizes have already been set. The size of each gate is a measure of the capacitance at each input in units of C, the capacitance of a unit sized transistor. Assume that the input B is random and uniformly distributed, that P_A=0.7 and that P_C=P_D=0.2.



1. For each node in the circuit, determine the probability P that the node is equal to '1' (6 pts)
2. Determine activity factor α for each node in circuit (8 pts)
3. What is the capacitance at each node in the circuit (ignoring internal gate nodes) in units of C? (11 pts)
4. If C (unit sized transistor) = 1.1 fF and V_{DD}=2.5V, what is dynamic power dissipation when running at 650 MHz ? (5 pts)