EE 471: Transport Phenomena in Solid State Devices

CMOS/SPICE Simulation Project

Due: 5/3/18

In this project you will be using the *LTspice* circuit simulator to investigate the properties of simple CMOS circuits and see how they compare with the properties that would be predicted using the material we have studied in this course.

You are responsible for proposing your own project. You can choose one of the suggestions below, or you can propose a project of your own design. In order to simulate your CMOS circuit, you should use the 180nm CMOS device models that you downloaded in HW 7. If you wish to propose a project of your own design, let me know what it is, so I can make sure there are no unforeseen problems in what you are proposing.

Note: Please do not use the schematic editor in *LTspice* to create your SPICE netlist. I want you to generate the SPICE code yourself, so that you learn how to use this language to describe circuits.

You will write a project report which will include a description of what it is that you are investigating, circuit schematics, SPICE code, screen shots of simulations and graphs of measured data vs. various parameters. Make sure your screen shots are readable. You can adjust colors, thickness of signal waveforms etc. in the *LTspice* user interface. In order to complete some projects, you may have to use commands that have not been described in our short lecture on SPICE. A comprehensive *LTspice* manual is available on the *Resources* page of the course website. If you are confused by the manual and not sure how to make the simulator perform some task, I am always available to answer your questions by email or stopping by my office.

Projects will be evaluated on their difficulty, the quality of the results you obtain and the clarity and completeness of their presentation in your report.

A few hints:

1. If you are performing a transient analysis, make sure the time-step is short enough to accurately capture the delays, rise-times or periods that you are trying to measure.
2. If you are trying to measure the delay of a circuit, make sure that your input waveforms have rise & fall times that are short compared to the delay you are measuring, otherwise they will determine the delay rather than the circuit you are measuring.
3. The 180nm process is nominally a 3.3V process. Do not use voltages larger than 5V – the models will not be reliable above 5V.
4. You can vary temperatures between -40ºC and 150ºC. Taking the temperature above 150 ºC would probably damage the real-world circuit.

5. The minimum gate length for this process is 180nm. But you can take the gate length down to 100nm if you are trying to study short channel effects.

Here are some possible projects you might choose:

1. A ring oscillator consists of an odd number (5 or greater) of inverters connected in a loop (the output of the last inverter drives the input of the first). Model a ring oscillator and measure the frequency of oscillation. How does the frequency change as a function of temperature and supply voltage? What happens if you put a heavy capacitive load on one of the outputs?
2. Plot the sub-threshold drain current of a MOS transistor vs. Vgs. The drain current should be shown on a log axis. Identify the sub-threshold and normal operating regions. Determine the sub-threshold slope (mV/decade) and the factor η. How do these values vary as a function of gate length? Try varying the gate length from 100nm to 500nm.
3. Model an 8-input NAND gate driving a 10fF load and determine the rising and falling delay from each input to the output. Use the following dimensions for a size 8 NMOS and size 2 PMOS transistor to properly account for diffusion capacitance:

   MN1 D G S B NMOS L=0.18um W=3.2um AD=1.2E-12 AS=1.2E-12 PD=7.2um PS=7.2um

   MP1 D G S B PMOS L=0.18um W=0.8um AD=3.2E-13 AS=3.2E-13 PD=2.4um PS=2.4um

   Compare the relative delays to what you would expect from Elmore delay analysis (Lecture 12). Now change the output load capacitance to 1pF and estimate the effective resistance (R) of a conducting unit transistor (L=0.18um, W=0.4um) from the data you have collected.
4. Investigate short channel effects in this process. Compare transistor curves for L=100nm to L= 500nm. How much more current do you get at L=100nm compared to L=500nm. How does this compare to what you would expect from the first order model? Determine the channel length modulation parameter as a function of gate length.
5. Determine the energy-delay product (Lecture 13) of a simple inverter driving a 100fF load (by measuring power supply current and delay) as a function of power supply voltage. At what value of supply voltage is this metric minimized? Does the optimum power supply value vary with gate length?
6. Plot the transfer function of a simple inverter. Determine the switching point and the high and low noise margins. How do these vary as a function of P/N width ratio?
7. Model a D (master-slave) flip-flop. Determine its dynamic performance parameters (delay from clock to Q and Qb, and minimum setup and hold times) as a function of supply voltage and temperature. Use an output load of 200 fF.