Lecture 1

Introduction to Solid State Electronics

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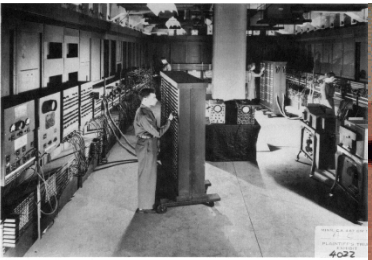
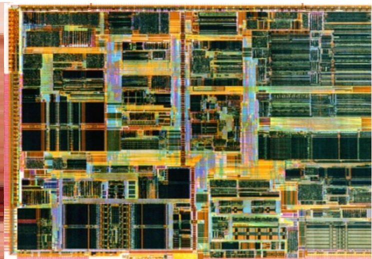
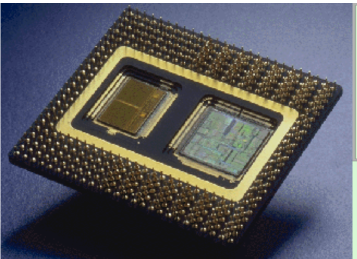
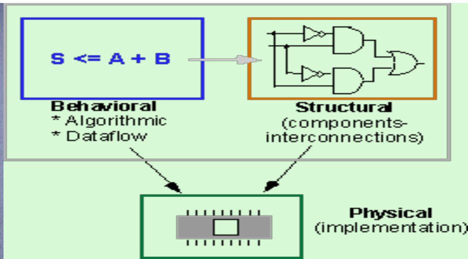


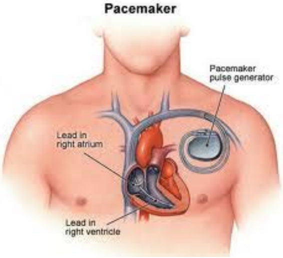






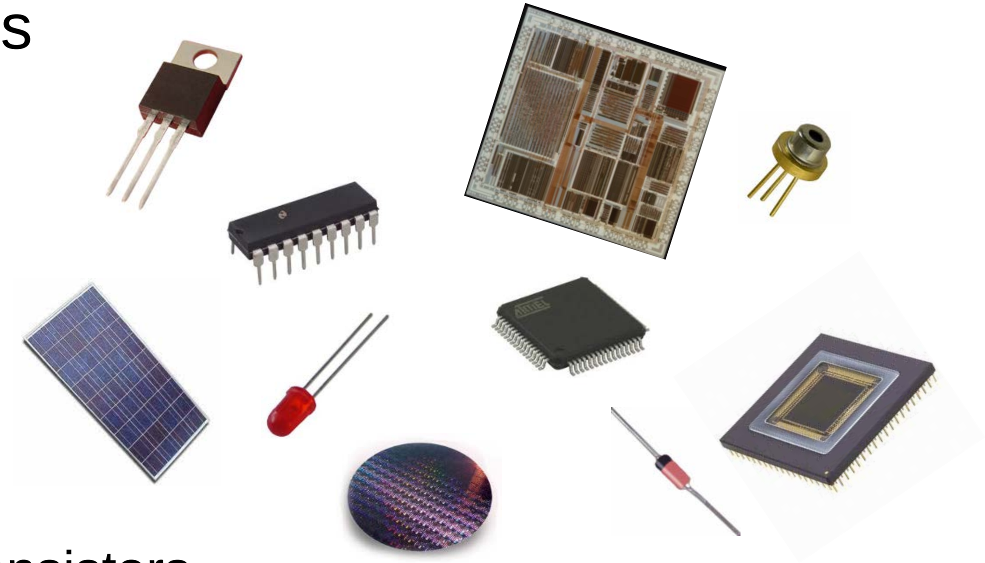
Ubiquity of Solid State Electronics

All enabled by incredibly small, rugged, high performance, low power solid state (semiconductor) electronics



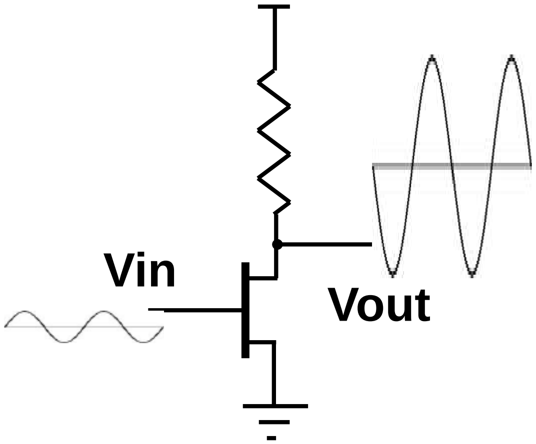
Solid State Devices

- Electronic systems consist of thousands (often millions, sometimes billions) of active solid state electronic components
  - diodes
  - bipolar transistors
  - MOS transistors
  - photo-detectors
  - LEDs, lasers
  - solar cells
  - flash (floating gate) transistors



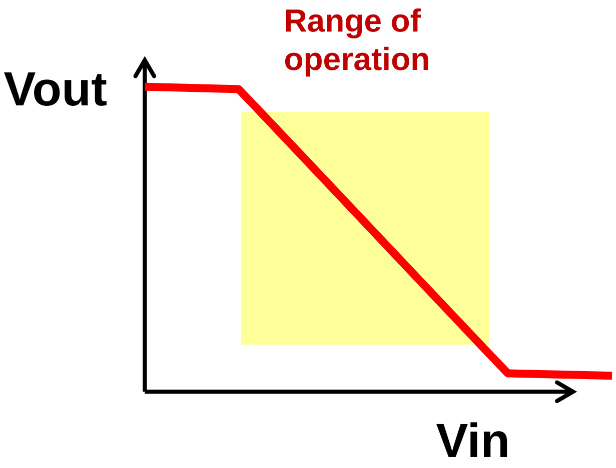
- Each of these active components exhibits a non-linearity which can be used to respond to, control and amplify electrical signals

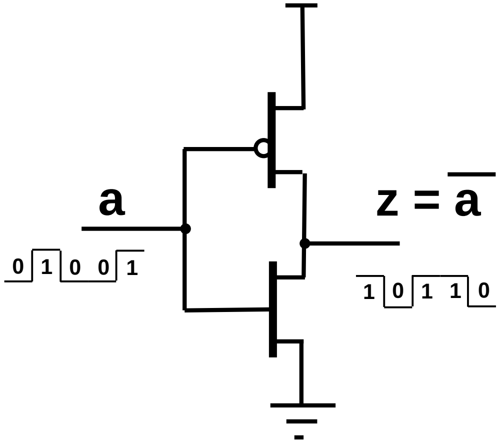
Analog & Digital Amplification



ANALOG

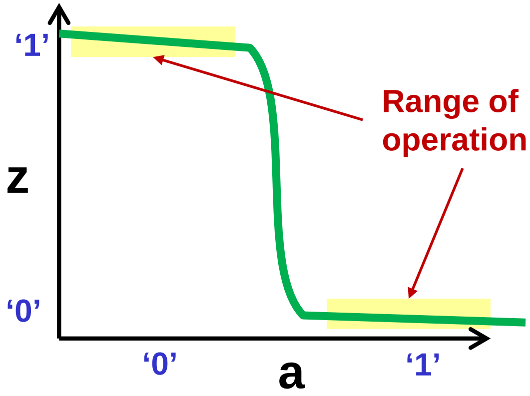
Circuit voltage represents continuous signal





DIGITAL

Circuit voltage represents one of two states: ‘0’ and ‘1’

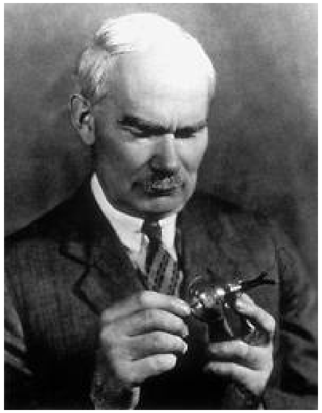


MIXED SIGNAL: Analog and digital in same circuit (chip)

Electronic Amplification – Vacuum Tube

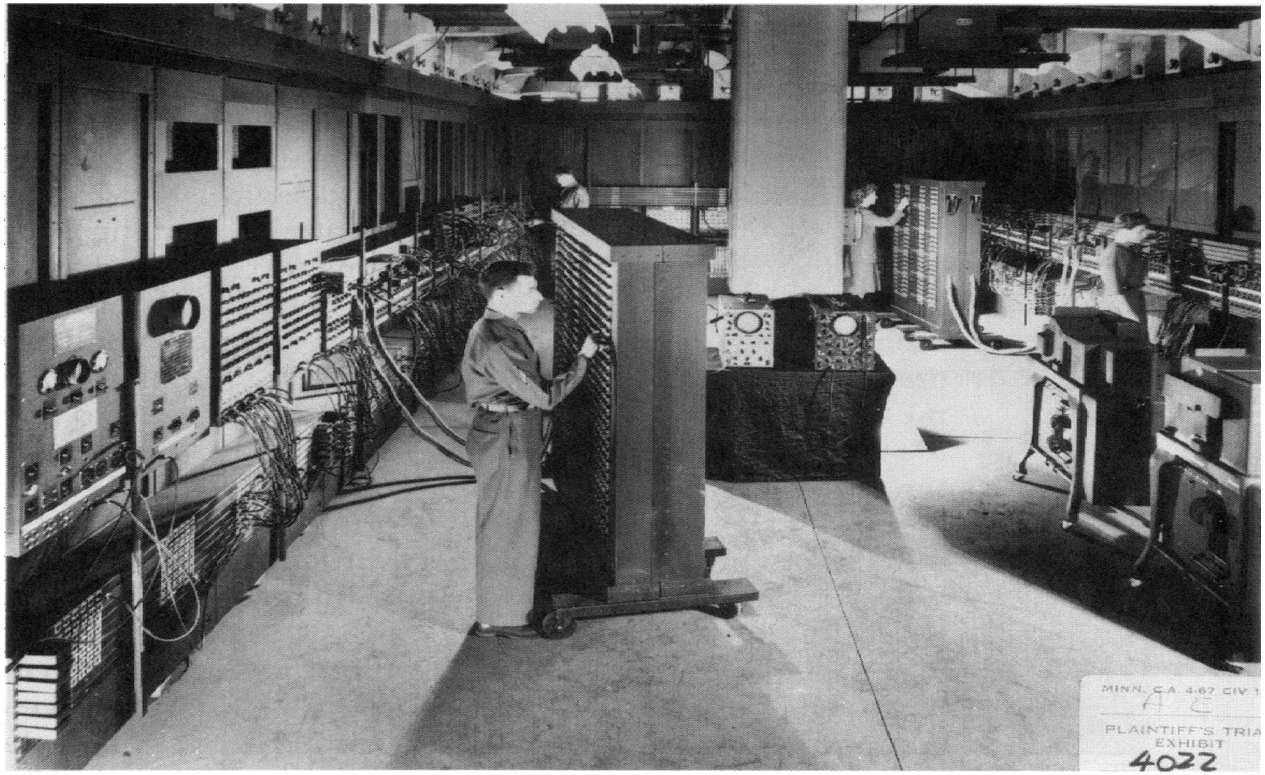
- Diode: John Fleming 1904
  - signal rectification

- Triode: Lee DeForest 1907
  - first electronic amplifier



- Used mainly in analog applications:
  - radio, TV, communication, radar, telephone networks
  - limited by size, power, fragility, microphonics and lifetime

ENIAC - The first electronic computer (1946)



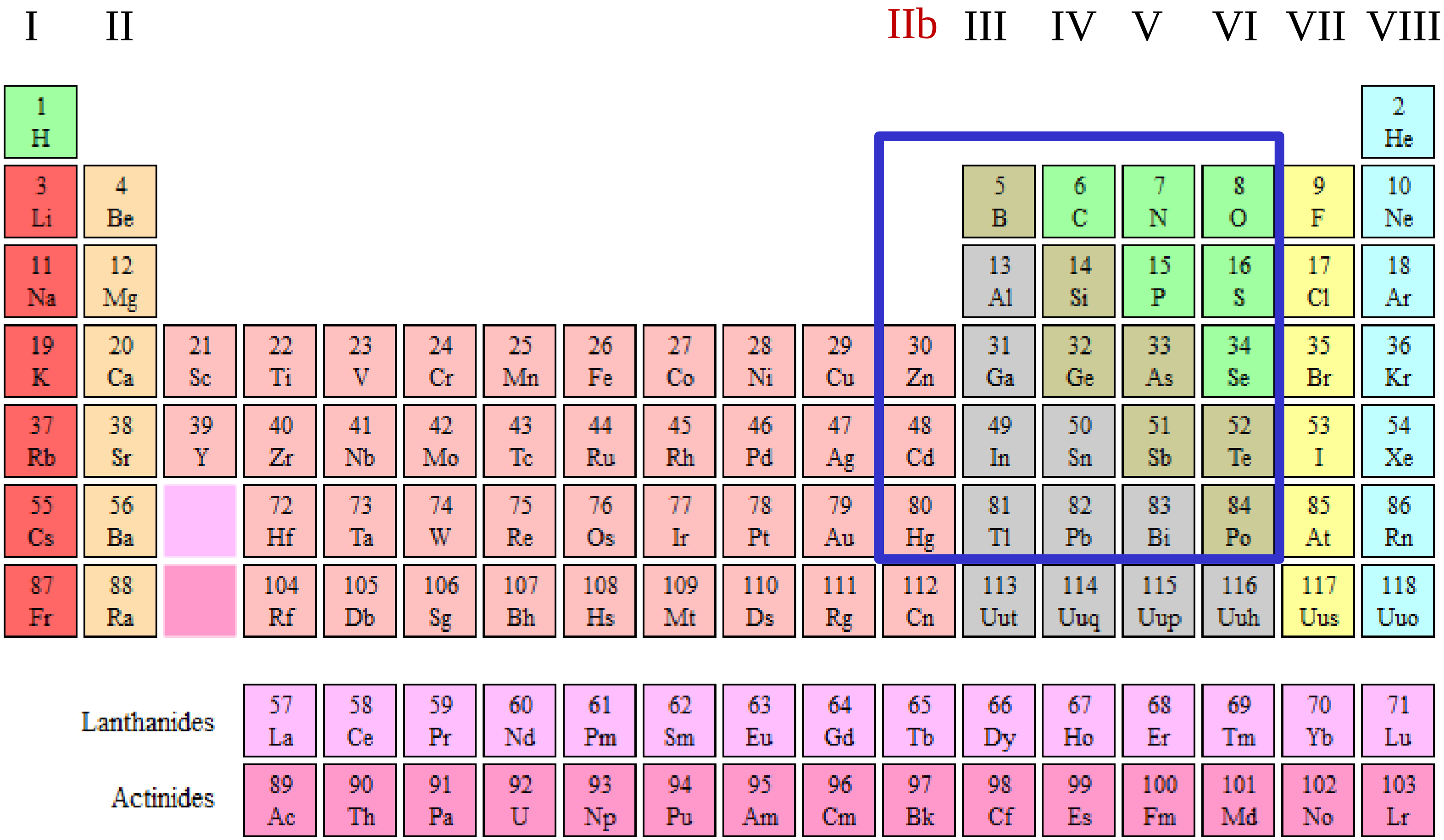
- 100 kHz clock
- 20 words memory
  (~ 100 bytes)
- 5000 operations/sec

10 feet tall, 30 tons 1,000 square feet of floor- space

More than 70,000 resistors
10,000 capacitors
6,000 switches
18,000 vacuum tubes

Requires 150 kilowatts of power;

Periodic Table & Semiconductors



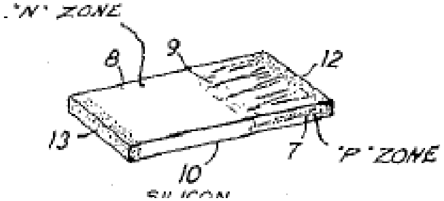
I	II										IIb	III	IV	V	VI	VII	VIII
1 H																	2 He
3 Li	4 Be											5 B	6 C	7 N	8 O	9 F	10 Ne
11 Na	12 Mg											13 Al	14 Si	15 P	16 S	17 Cl	18 Ar
19 K	20 Ca	21 Sc	22 Ti	23 V	24 Cr	25 Mn	26 Fe	27 Co	28 Ni	29 Cu	30 Zn	31 Ga	32 Ge	33 As	34 Se	35 Br	36 Kr
37 Rb	38 Sr	39 Y	40 Zr	41 Nb	42 Mo	43 Tc	44 Ru	45 Rh	46 Pd	47 Ag	48 Cd	49 In	50 Sn	51 Sb	52 Te	53 I	54 Xe
55 Cs	56 Ba		72 Hf	73 Ta	74 W	75 Re	76 Os	77 Ir	78 Pt	79 Au	80 Hg	81 Tl	82 Pb	83 Bi	84 Po	85 At	86 Rn
87 Fr	88 Ra		104 Rf	105 Db	106 Sg	107 Bh	108 Hs	109 Mt	110 Ds	111 Rg	112 Cn	113 Uut	114 Uuq	115 Uup	116 Uuh	117 Uus	118 Uuo
Lanthanides			57 La	58 Ce	59 Pr	60 Nd	61 Pm	62 Sm	63 Eu	64 Gd	65 Tb	66 Dy	67 Ho	68 Er	69 Tm	70 Yb	71 Lu
Actinides			89 Ac	90 Th	91 Pa	92 U	93 Np	94 Pu	95 Am	96 Cm	97 Bk	98 Cf	99 Es	100 Fm	101 Md	102 No	103 Lr

History of Solid State Devices

- Cat’s Whisker - Jagadish Bose (1901)
    - thin metal wire in contact with semiconductor crystal (PbS, SiC)
    - point contact diode (primitive Schottky)
    - used as radio detector
    - did not understand how it worked

- Junction Diode – Russel Ohl (1940)
    - observed photoelectric effect and rectifying properties of silicon rod
    - explained operation in terms of “P-N barrier”

FIG. 2



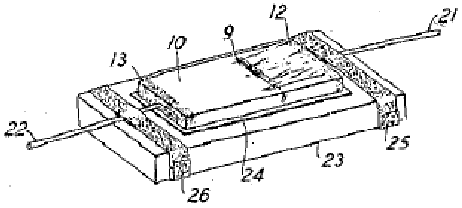


FIG. 5

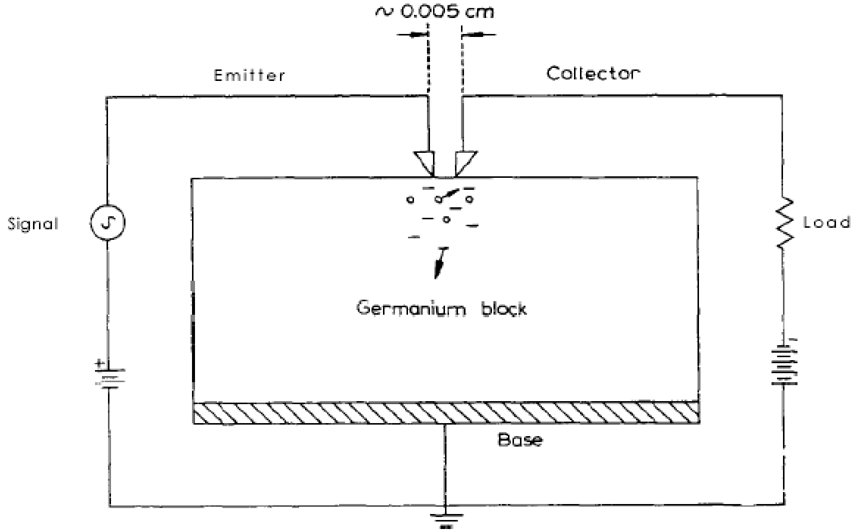
from Russel Ohl patent application “light sensitive electric device”

Transistor Age…

1947: Bardeen and Brattain create point-contact transistor

First solid state amplifying device (gain=18)

but not manufacturable

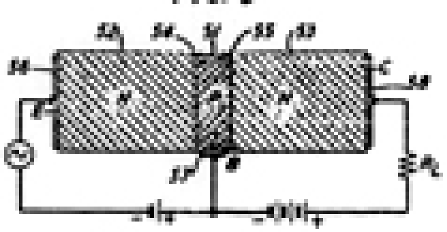


Junction Transistor

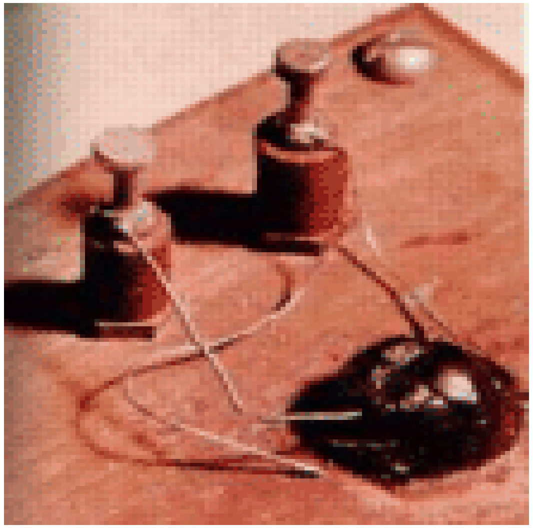
1948: Shockley develops idea of a sandwich junction transistor

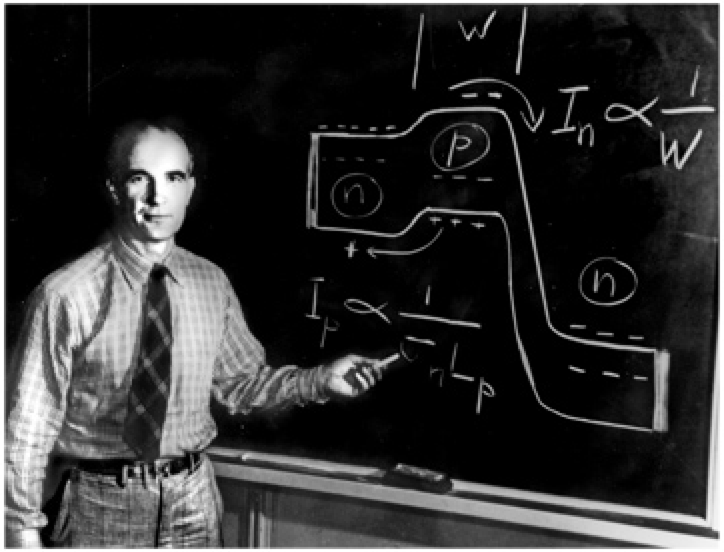
- based on minority carrier injection

FIG. 3



1951: Bell Labs announces manufacturable germanium transistor using grown junctions

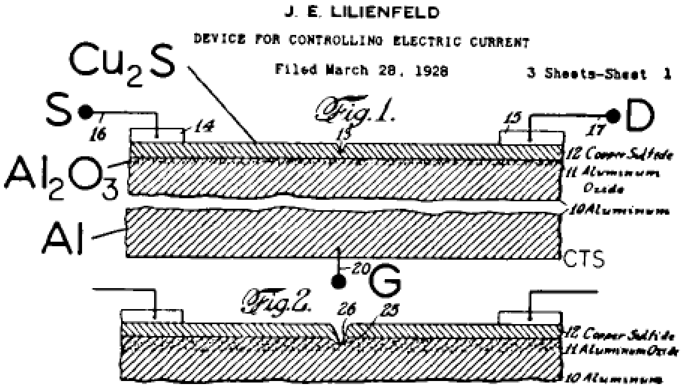




1954: Gordon Teal (Texas Instruments) develops first silicon junction transistor

MOS (Field Effect) Transistor

1926: Lilienfeld proposes and patents idea of controlling conduction through semiconductor film via a metal plate, separated from semiconductor by insulating layer

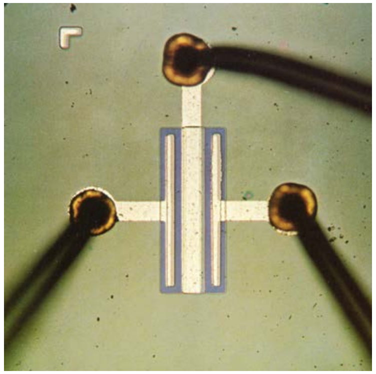


1945: Shockley explores concept of field-effect transistor – unsuccessful experiments with Bardeen

1960: Atallah & Khang (Bell Labs) demonstrate silicon MOS transistor

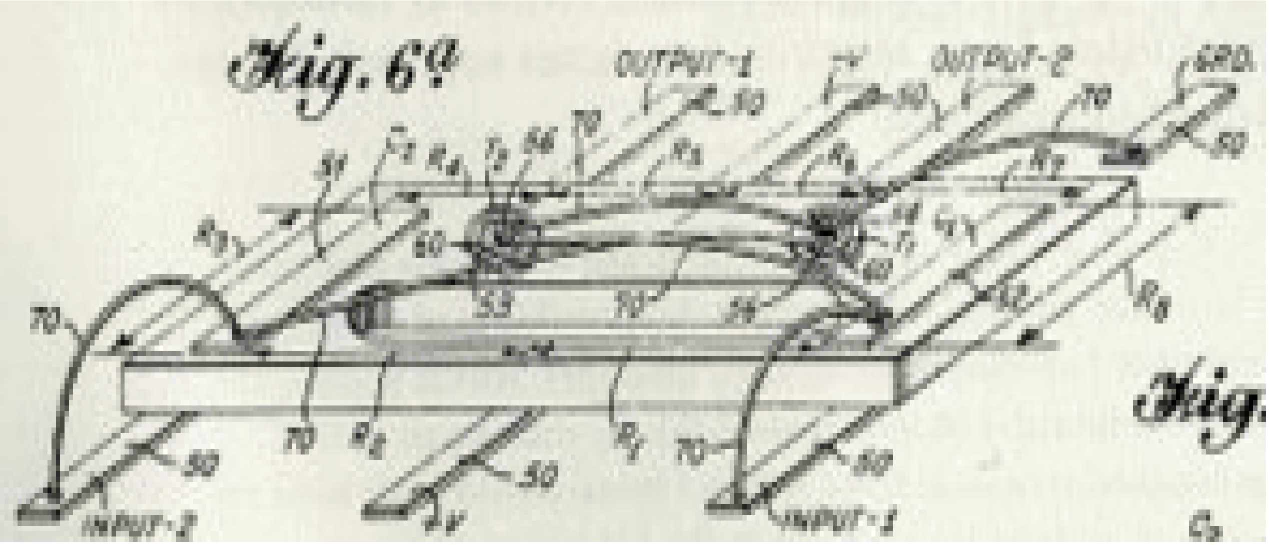
- low gain, slow

- recognized ease of manufacture



early Fairchild PMOS transistor

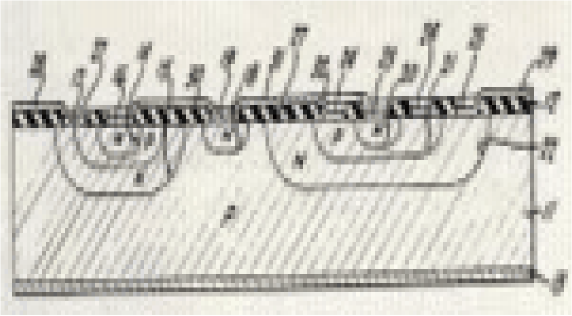
The Integrated Circuit

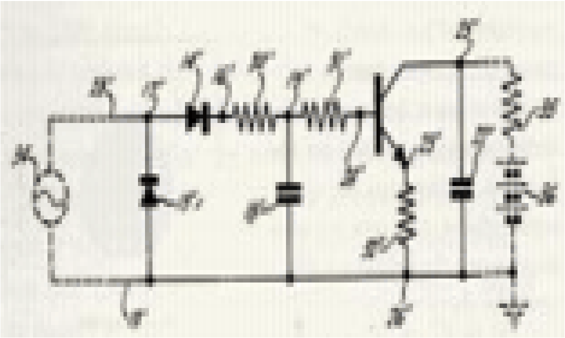


Jack Kilby, working at Texas Instruments, invented a monolithic “integrated circuit” in July 1959.

He constructed the flip-flop shown in the patent drawing above.

Planar transistors



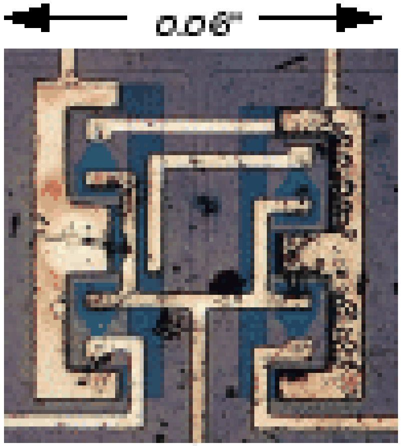


In mid 1959, Noyce develops the first true IC using planar transistors:

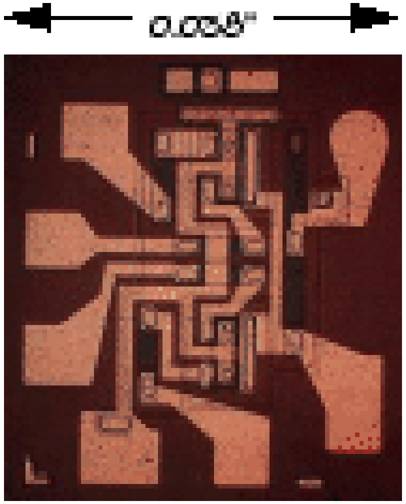
- Reverse biased pn junctions for isolation
- Diode-isolated silicon resistors and
- SiO_2 insulation
- Evaporated metal wiring on top

This enabled designers to place and connect multiple transistors on silicon die using sophisticated "printing process"

First Digital ICs – early 60’s

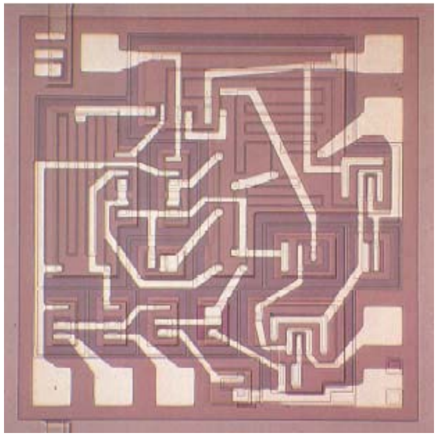


1961: TI and Fairchild introduced first logic IC’s: dual flip-flop with 4 transistors (cost ~$50)



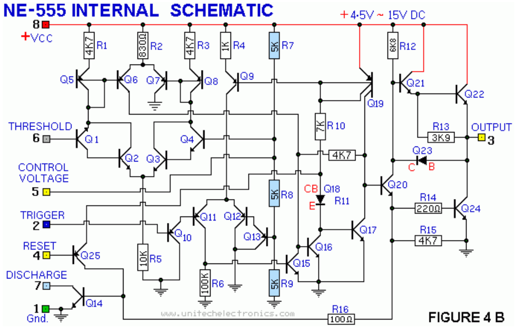
1963: Densities and yields improve. This circuit has four flip-flops.

Early Analog ICs



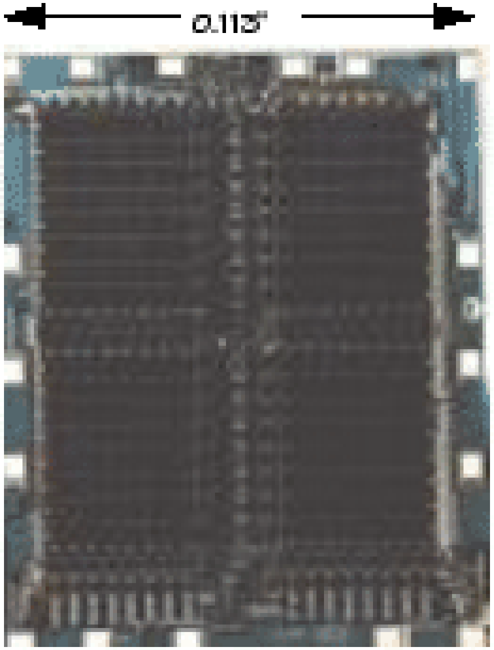
1965: Fairchild μA709 Operational Amplifier: 13 bipolar transistors, open loop gain 70,000

1968: Fairchild μA741 Operational Amplifier: 20 bipolar & 11 resistors *plus 30pF compensation capacitor*

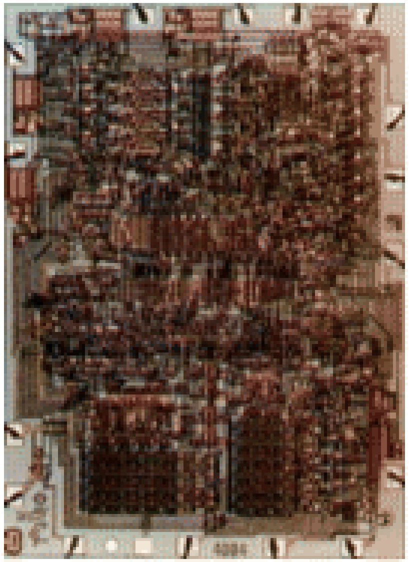


1971: Signetics 555 Timer: 24 transistors & 15 resistors

Continuing Development early 70’s



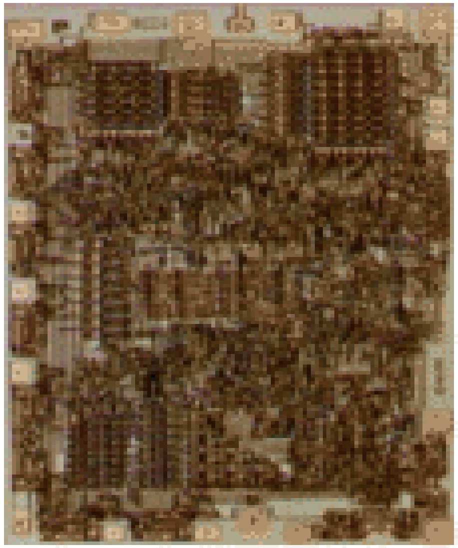
1970: Intel starts selling a 1k bit RAM.



1971: Ted Hoff at Intel designed the first microprocessor.

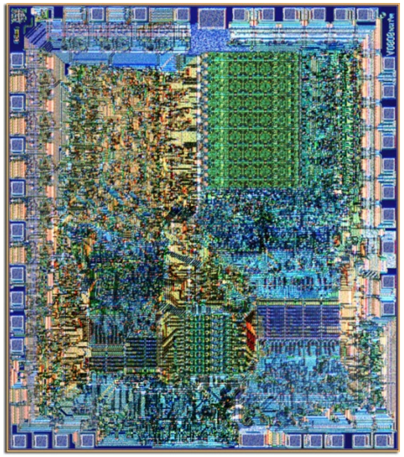
The 4004 had 4-bit busses and a clock rate of 108 KHz. It had 2300 transistors and was built in a 10 um process.

Continuing Development – Microprocessor



1972: 8008 introduced.

3,500 transistors supporting a byte-wide data path.



1974: Introduction of the 8080 – first “truly usable microprocessor”

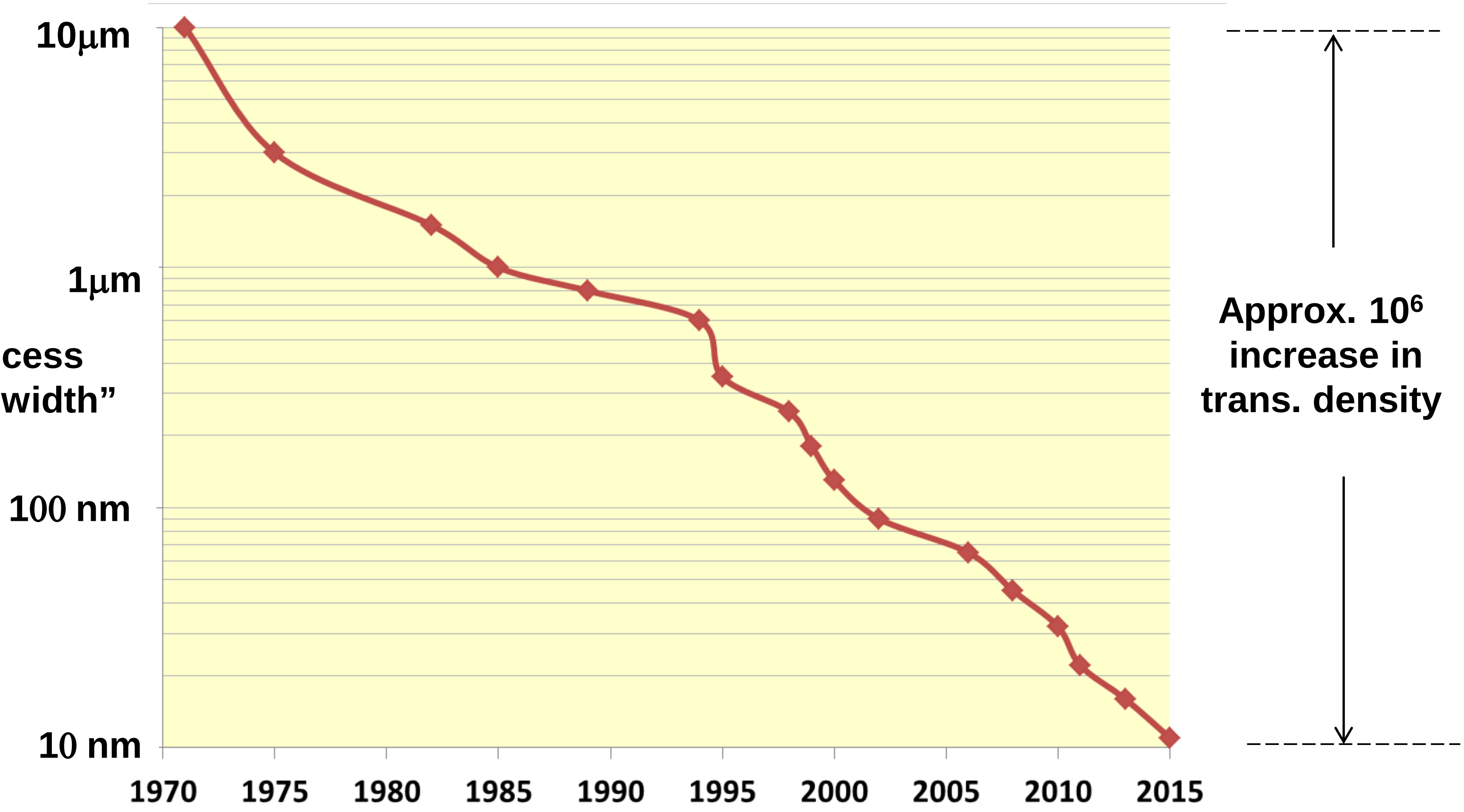
8-bit data, 16-bit address bus (up to 64kB memory)

6,000 transistors in a 6 um process.

Clock rate was 2 MHz.

Exponential Growth

Planar "printing process" enabled continuing reductions in process "line width" which has led to increased density in transistors/mm^2



Process "line-width"

Approx. 10^6 increase in trans. density

What has brought about this extraordinary growth?

Huge investments in and major advances in:

- Solid State Physics
- Materials Science
- Lithography and fab
- Device modeling

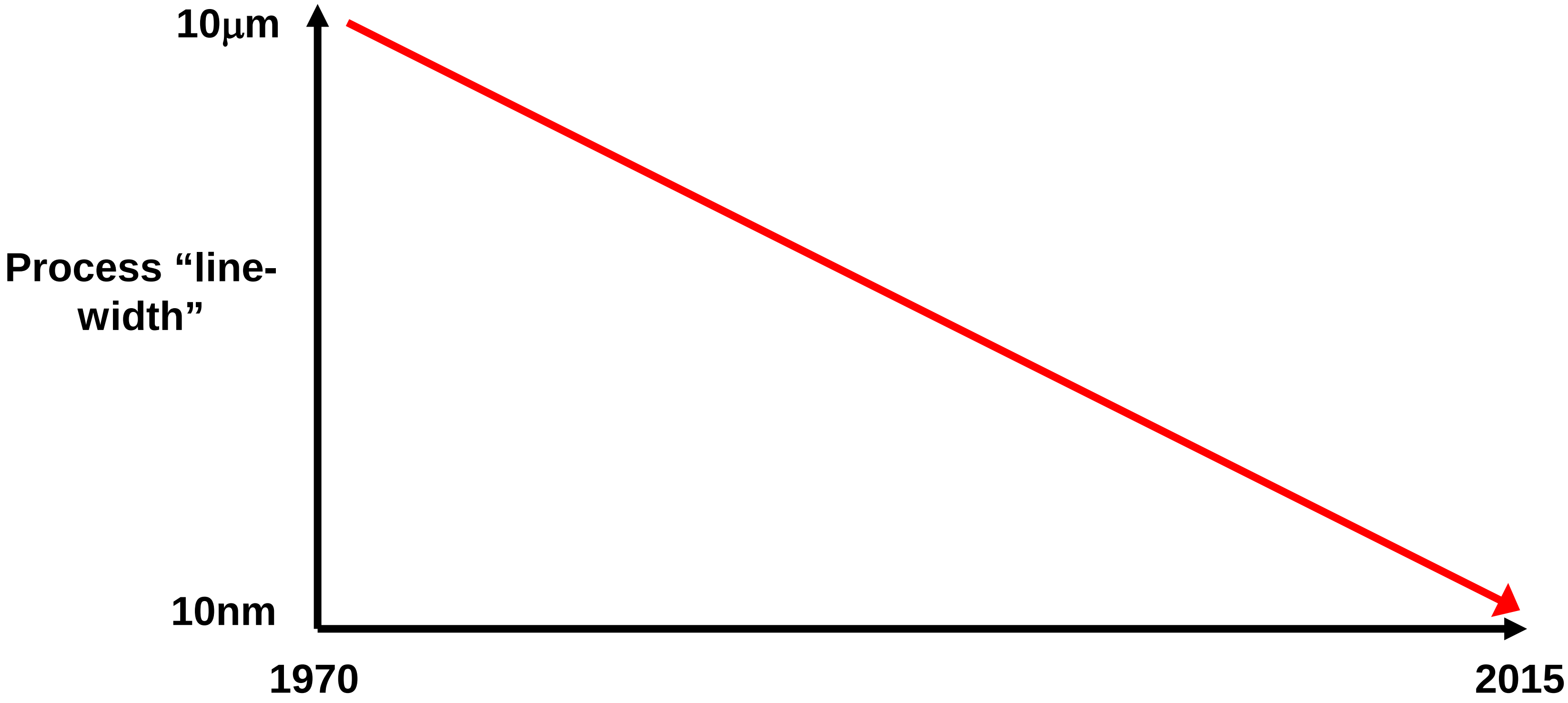
- Circuit design and layout
- Architecture design
- Algorithms
- CAD tools

Cost of building 65nm fab was around $3B !

Cost of building 22nm fab is around $7B !

Cost of building 10nm fab is around $12B !

Analog vs. Digital Revisited



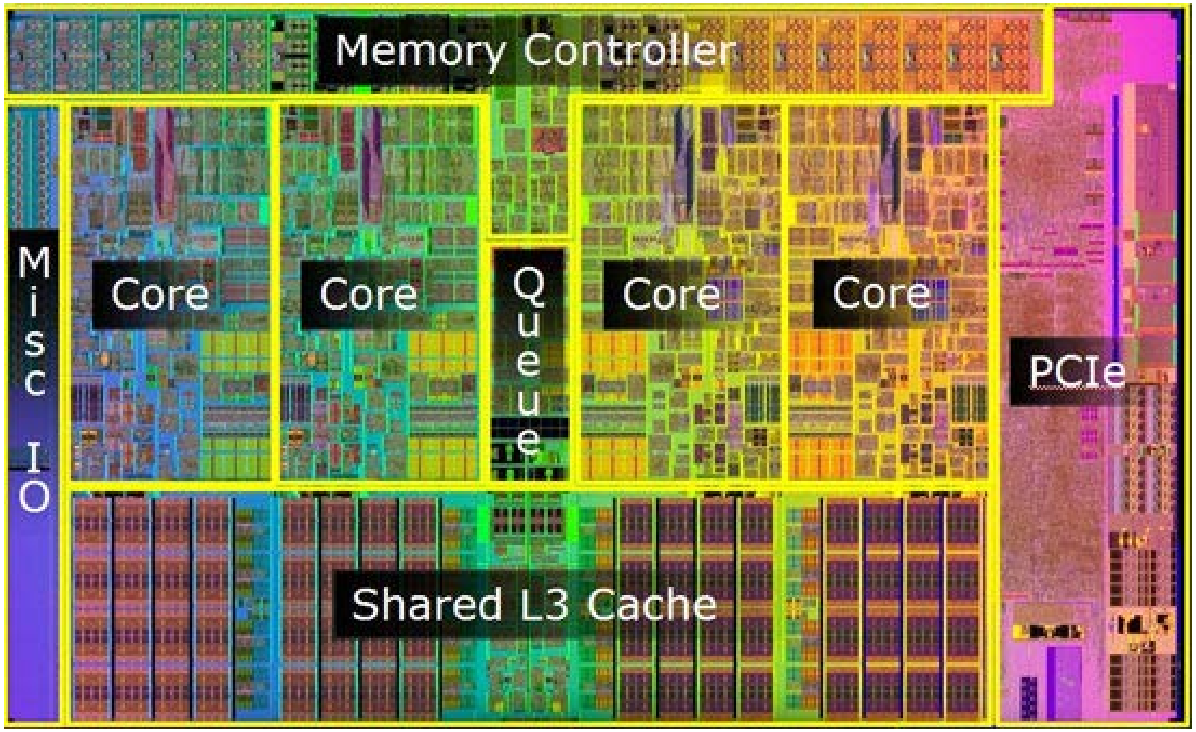
Few large transistors
High voltage (~15V)
Low speed
High power (per transistor)
"Ideal" transistor behavior

Well suited to analog

Many small transistors
Low voltage (~0.5V)
High speed
Low power (per transistor)
"Non-ideal" transistor behavior

Well suited to digital

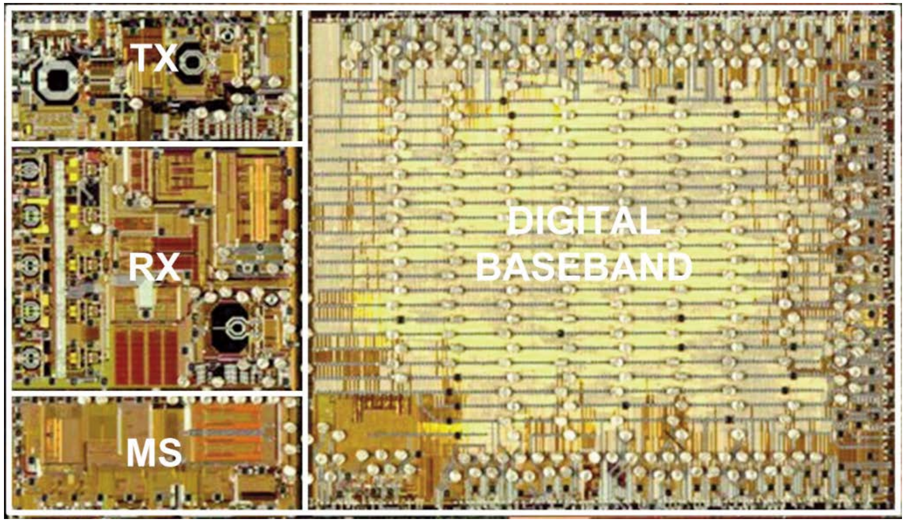
High Performance Digital: Intel i5– 45 nm

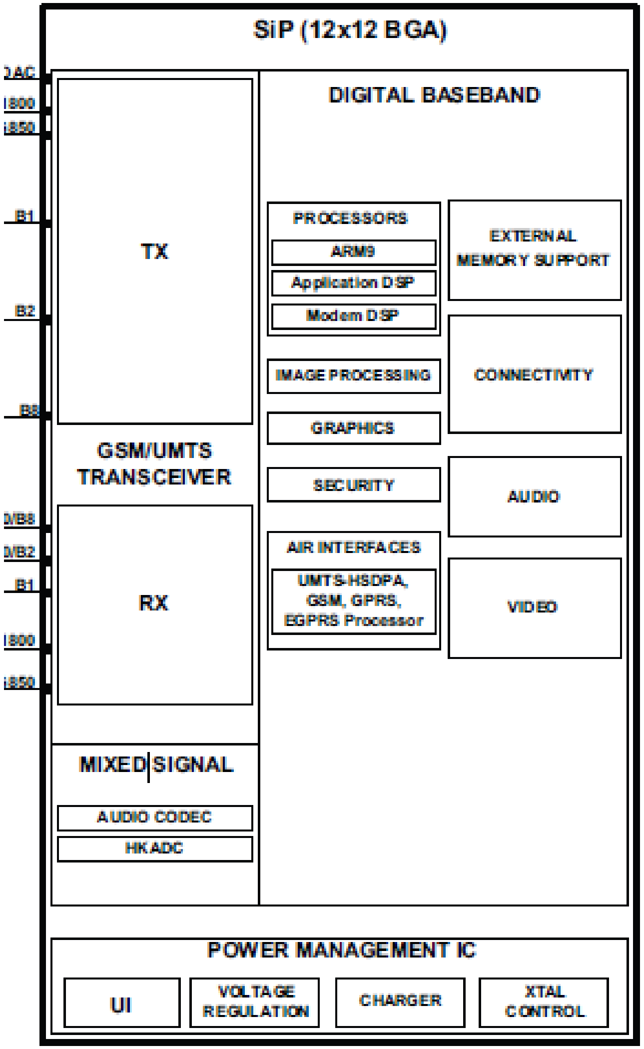


- Introduced 2009 (2.6 GHz)
- Level 3 cache: 8MB
- 4 cores / 4 threads
- Transistors: 774 Million
- 95 W

UMTS/GSM Transceiver with Digital Baseband

- Qualcom mixed-signal “system on chip”
  - RF transceiver
  - A/Ds, D/As
  - Digital baseband
  - Audio/Video codec
  - Multimedia processing
  - Power management
  - 65nm CMOS

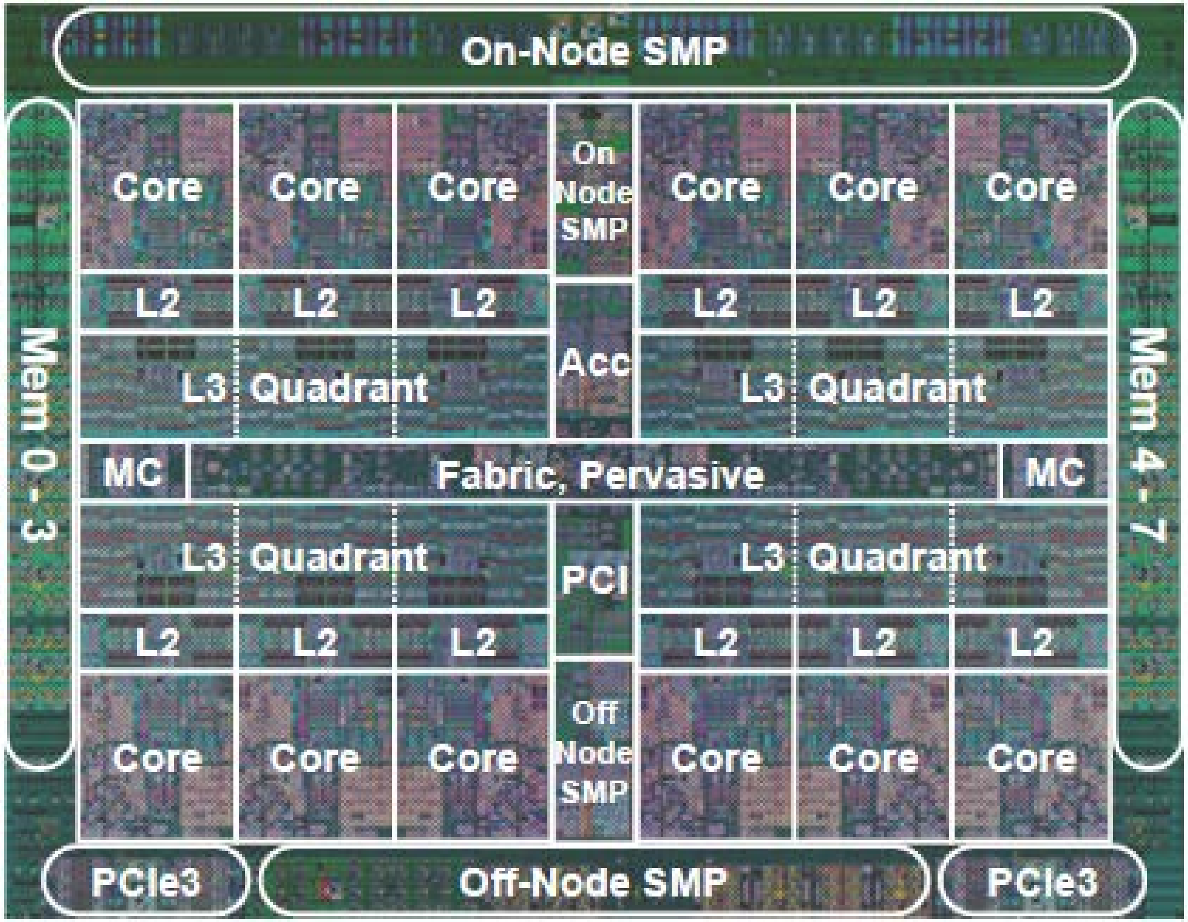




IEEE ISSCC 2011

IBM Server Class Microprocessor

- 22 nm SOI process
- 12 cores 4.5 GHz
- 4.2B transistors
- 6 MB L2 / 96 MB L3
- 7.6 Tb/s I/O BW
- 649 mm^2 die

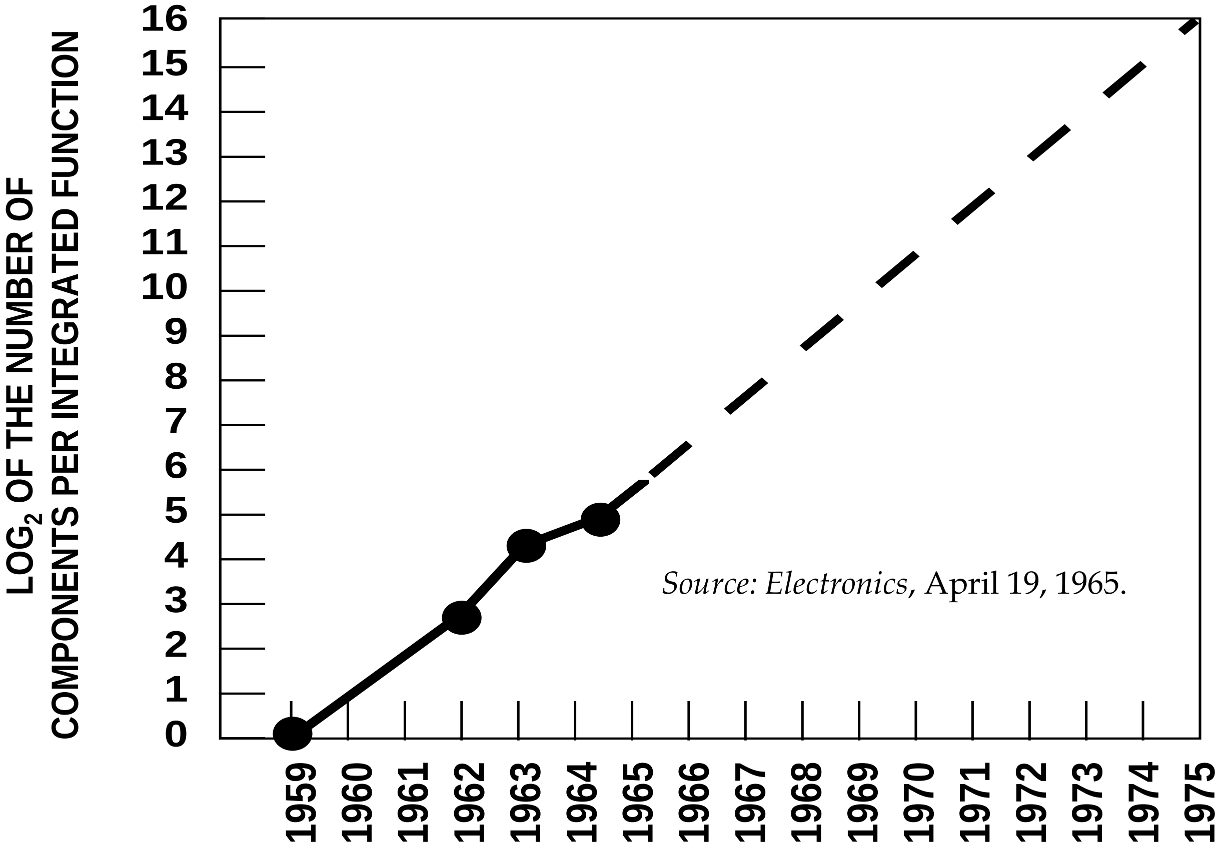


~ 1.1 inches

IEEE ISSCC 2014

Moore's Law

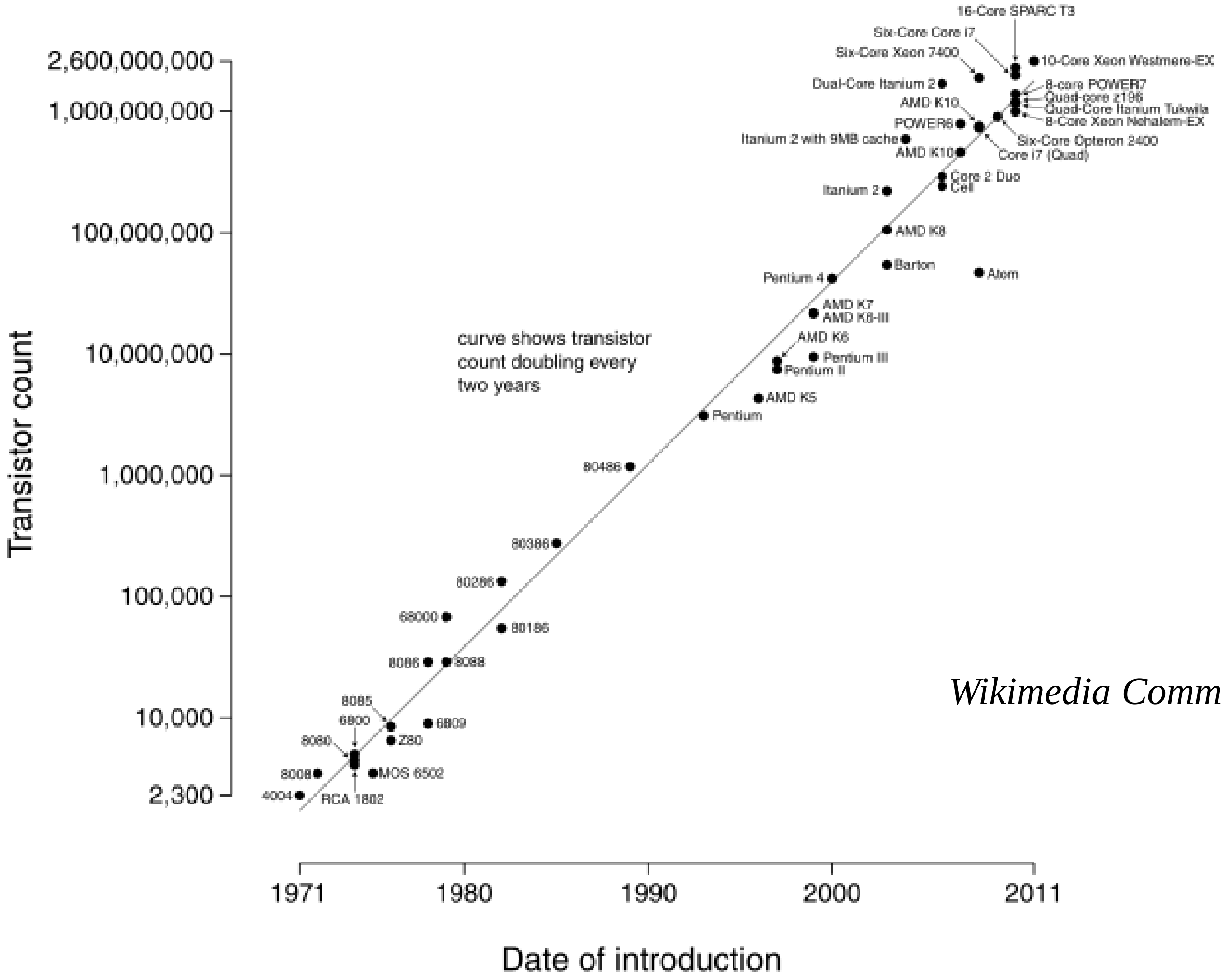
- In 1965, Gordon Moore noted that the number of transistors on a chip approximately doubled every 12 months.



Source: Electronics, April 19, 1965.

- He made a prediction that IC cost effective component count would continue to double every 12 months

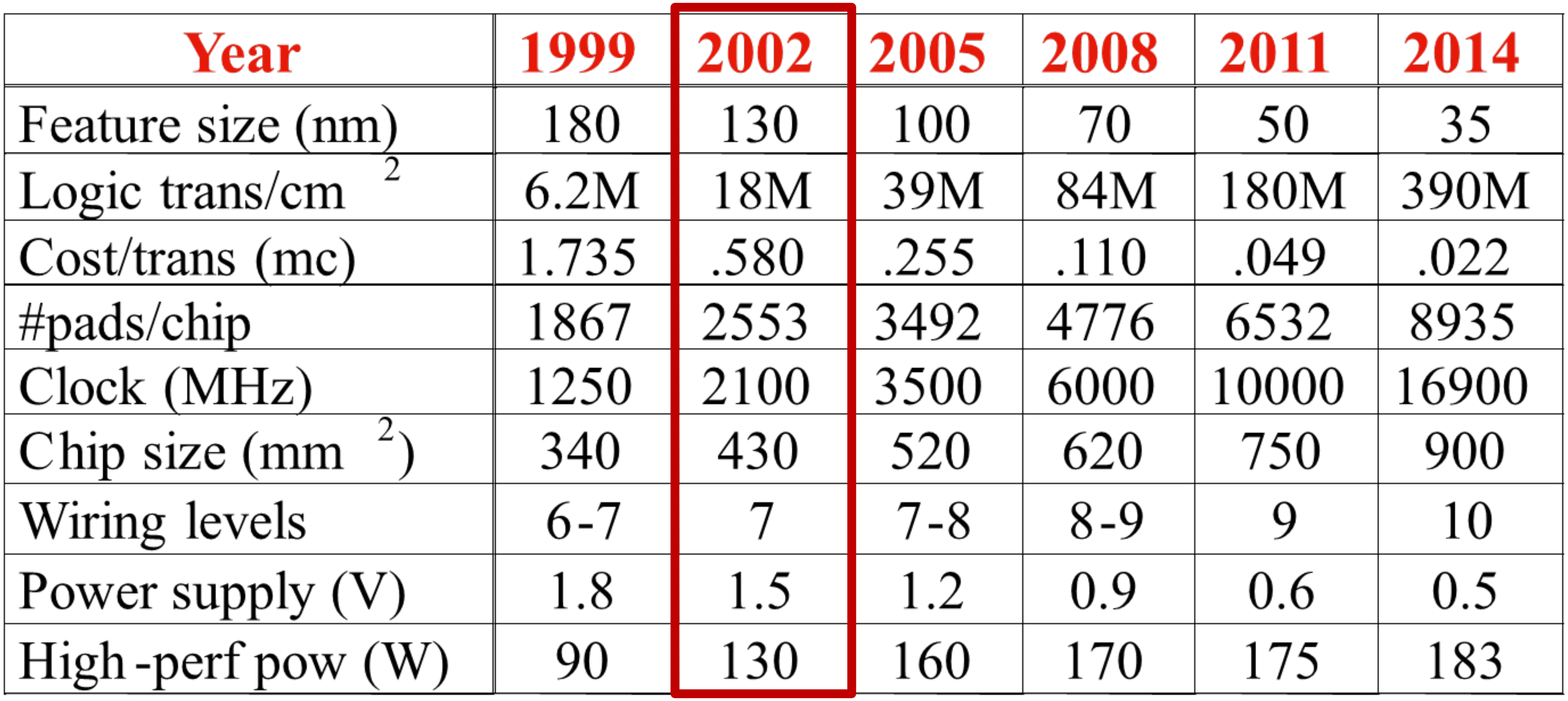
Moore’s Law – how it checked out



Wikimedia Commons 2011

- Actual growth has been a doubling every 18-24 months

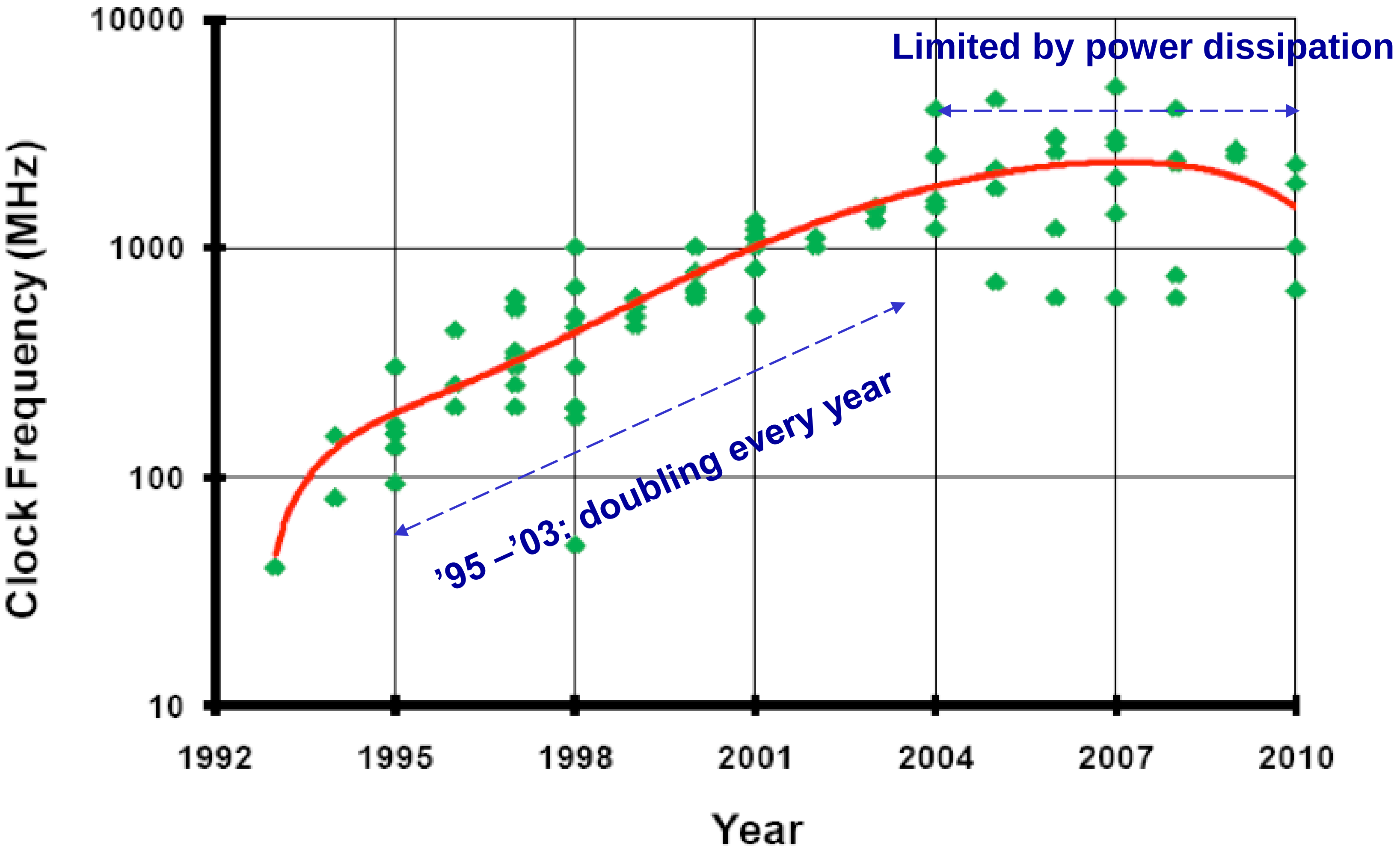
Technology Directions: SIA Roadmap



Year	1999	2002	2005	2008	2011	2014
Feature size (nm)	180	130	100	70	50	35
Logic trans/cm^2	6.2M	18M	39M	84M	180M	390M
Cost/trans (mc)	1.735	.580	.255	.110	.049	.022
#pads/chip	1867	2553	3492	4776	6532	8935
Clock (MHz)	1250	2100	3500	6000	10000	16900
Chip size (mm^2)	340	430	520	620	750	900
Wiring levels	6-7	7	7-8	8-9	9	10
Power supply (V)	1.8	1.5	1.2	0.9	0.6	0.5
High-perf pow (W)	90	130	160	170	175	183

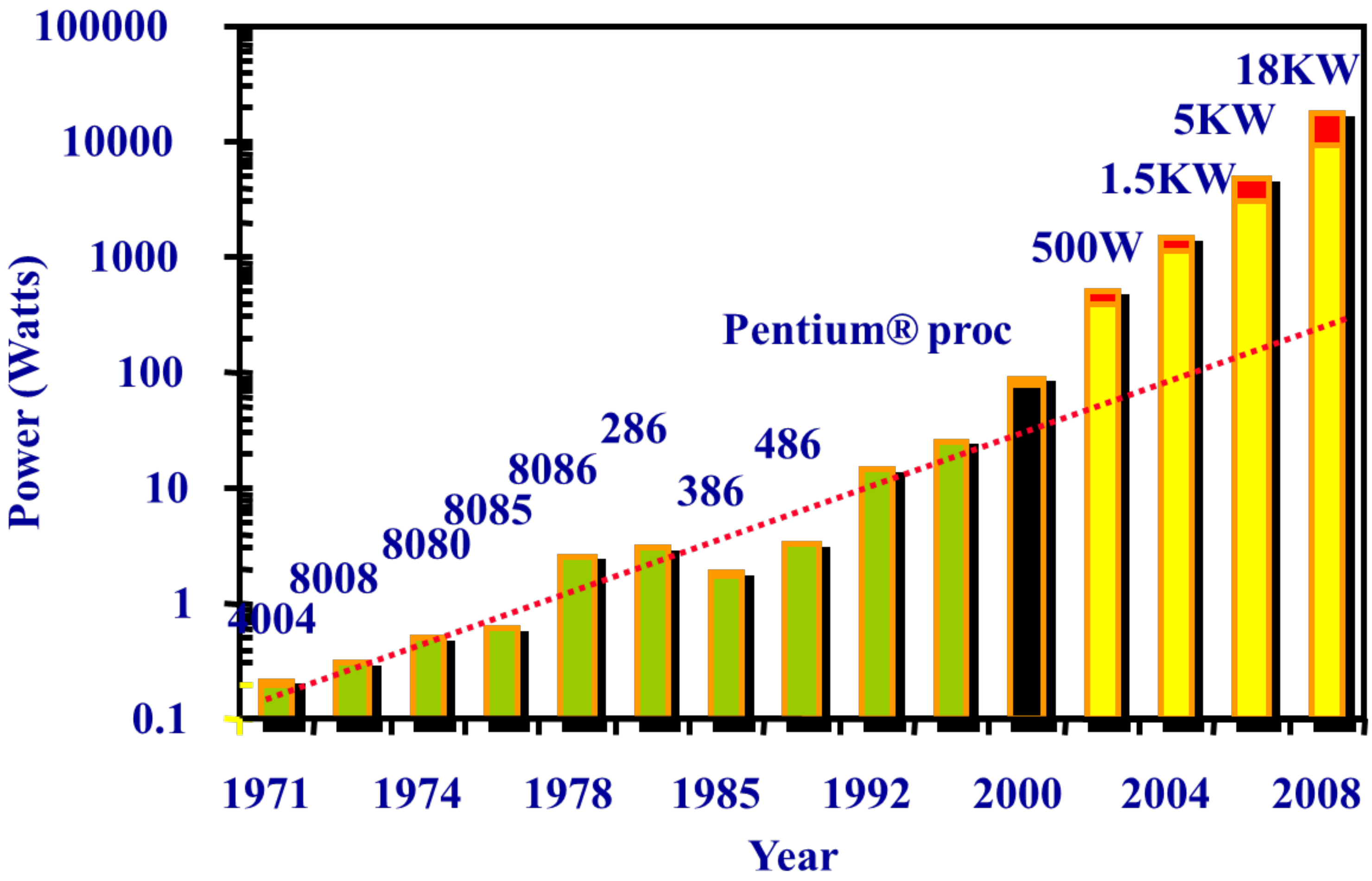
- Roadmap has become a self-fulfilling prophecy!

Microprocessor Clock Frequency



ISSCC Trends Report 2010

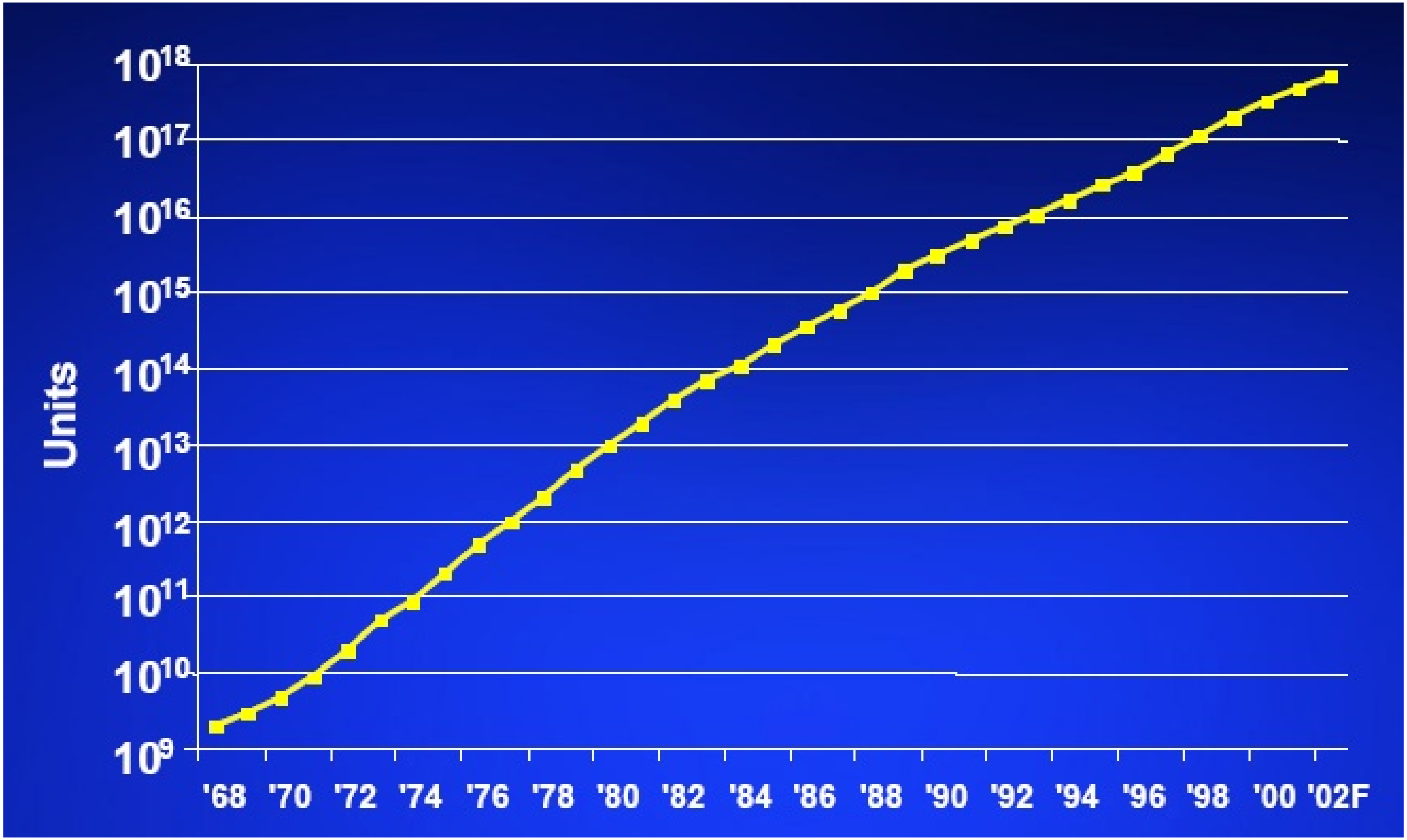
Microprocessor Power Projection 2000



- Increasing processing speed thru clock rate is power prohibitive
- Solution today is use of parallelism (#processors, #threads)

Courtesy, Intel

Transistors shipped per year

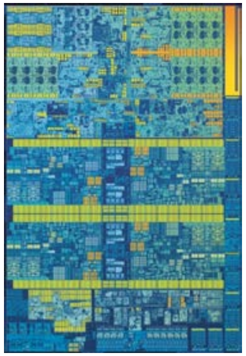


Source: Dataquest/Intel, 8/02

Decades of Progress

Intel 4004 Processor
(1978)

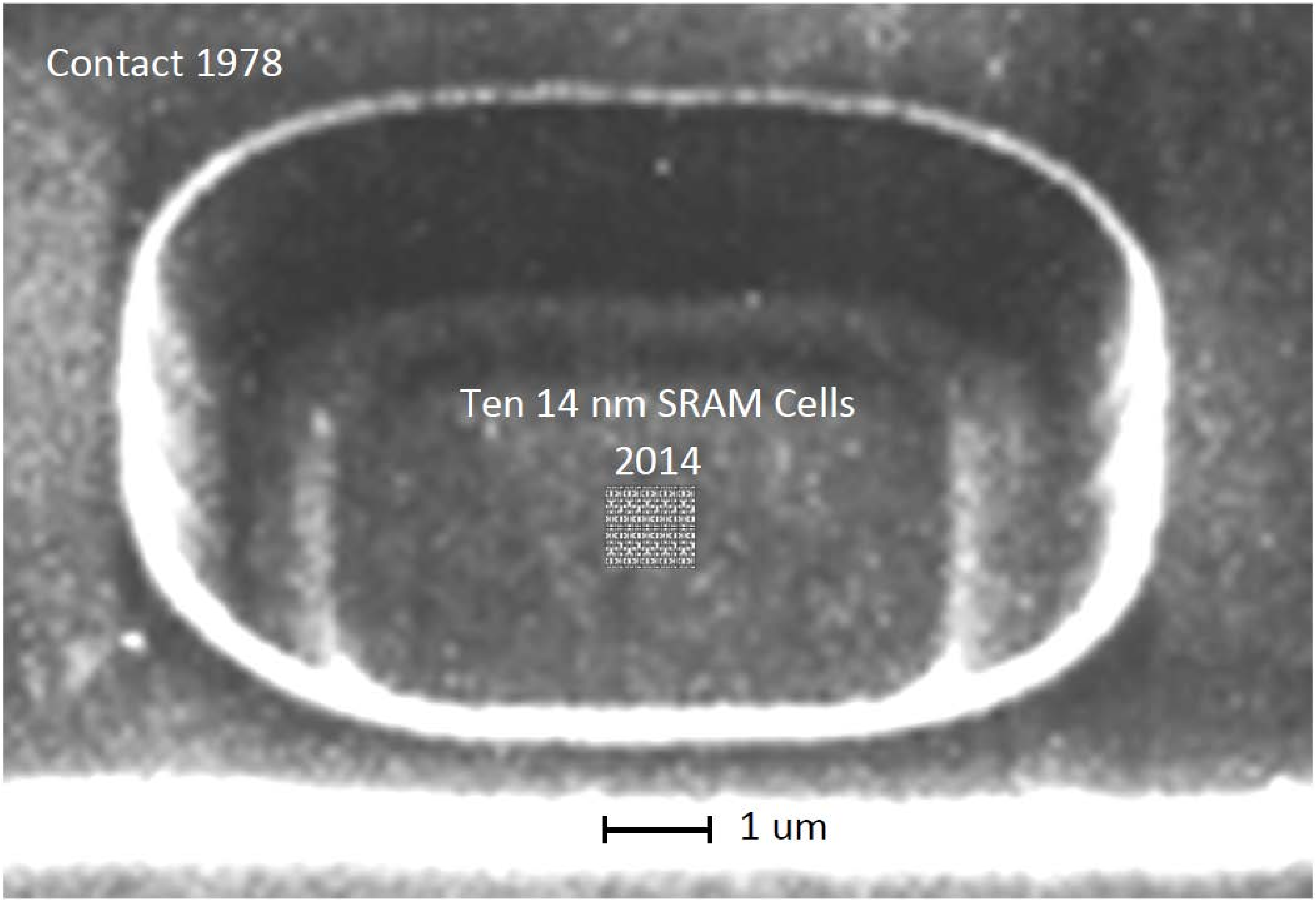
6th Generation Intel Core Processor (2015)



Processor		4004 to 14nm
Wafer Size	↑	36x area
Technology Linewidth	↓	700x
Performance	↑	3,500x
Price per Transistor	↓	60,000x
Transistor Energy Efficiency	↑	90,000x

Moore’s Law: A Path Forward. William Holt, ISSCC 2016

What does 700x Scaling Look Like?



Moore’s Law: A Path Forward. William Holt, ISSCC 2016

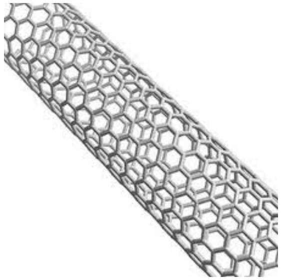
Where do we go from here?

- CMOS is reaching its physical limits
- ITRS projects 5nm technology in 2020
- Silicon crystal is 0.5nm – atoms are 0.2nm apart
- Gate oxides 5 Si atoms thick
- Quantum behavior
- Power dissipation and interconnect delays limit performance (not intrinsic device speed)

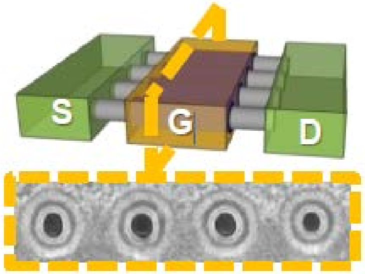
- BUT – prophets of CMOS demise have always been wrong

New technologies are being explored

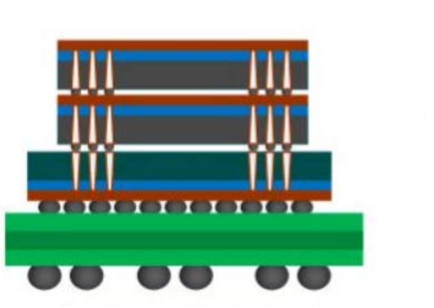
- carbon nanotubes (ballistic transport)



- spintronics (based in electron spin)
- Nanowire FET



- 3D-IC



- organic transistors
  - semiconducting polymers

- any new technology will require enormous investment to “catch-up” to CMOS