EE 471: Transport Phenomena in Solid State Devices

Spring 2018

Lecture 7
MOS Capacitor

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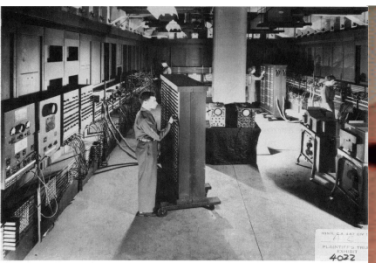
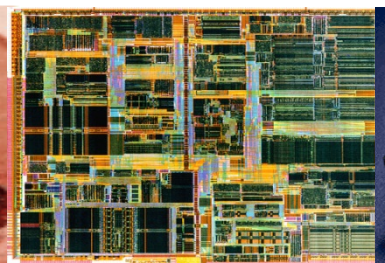
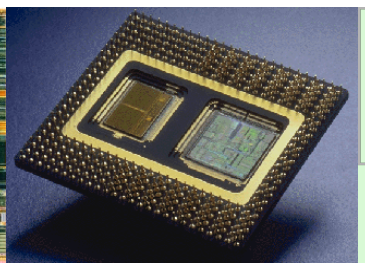
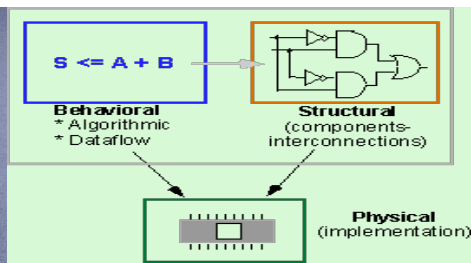
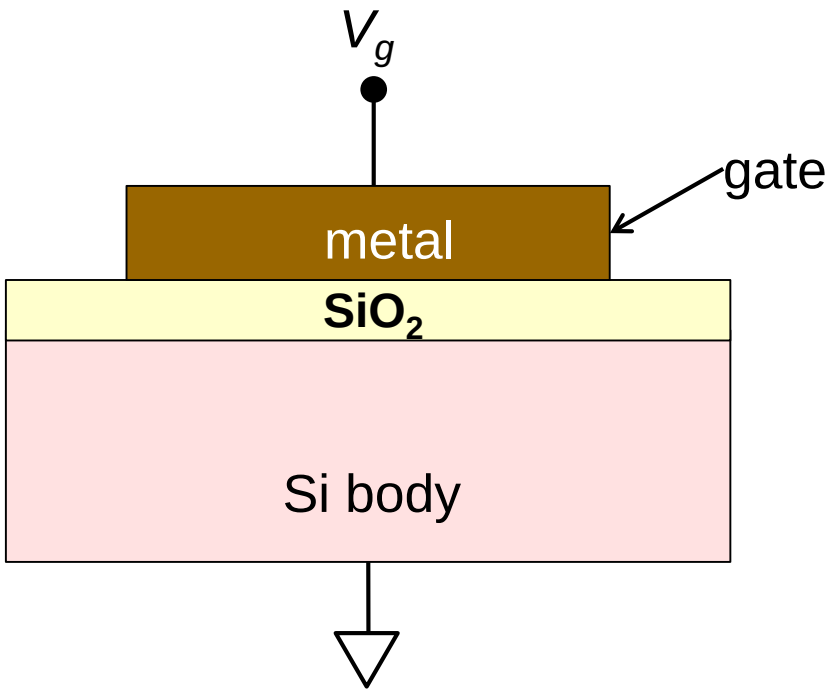
Adapted from Modern Semiconductor Devices for Integrated Circuits, Chenming Hu, 2010

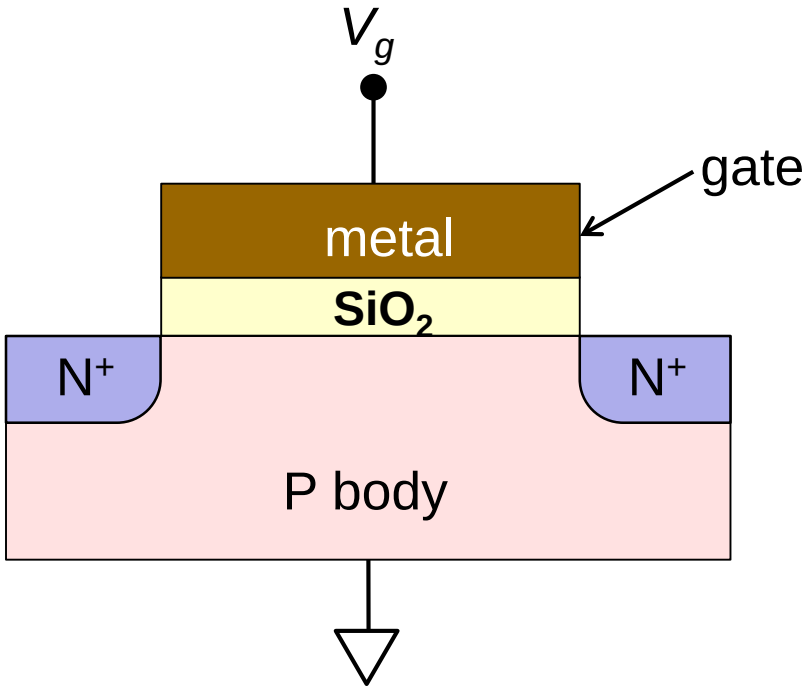


MOS Metal-Oxide-Semiconductor



MOS capacitor

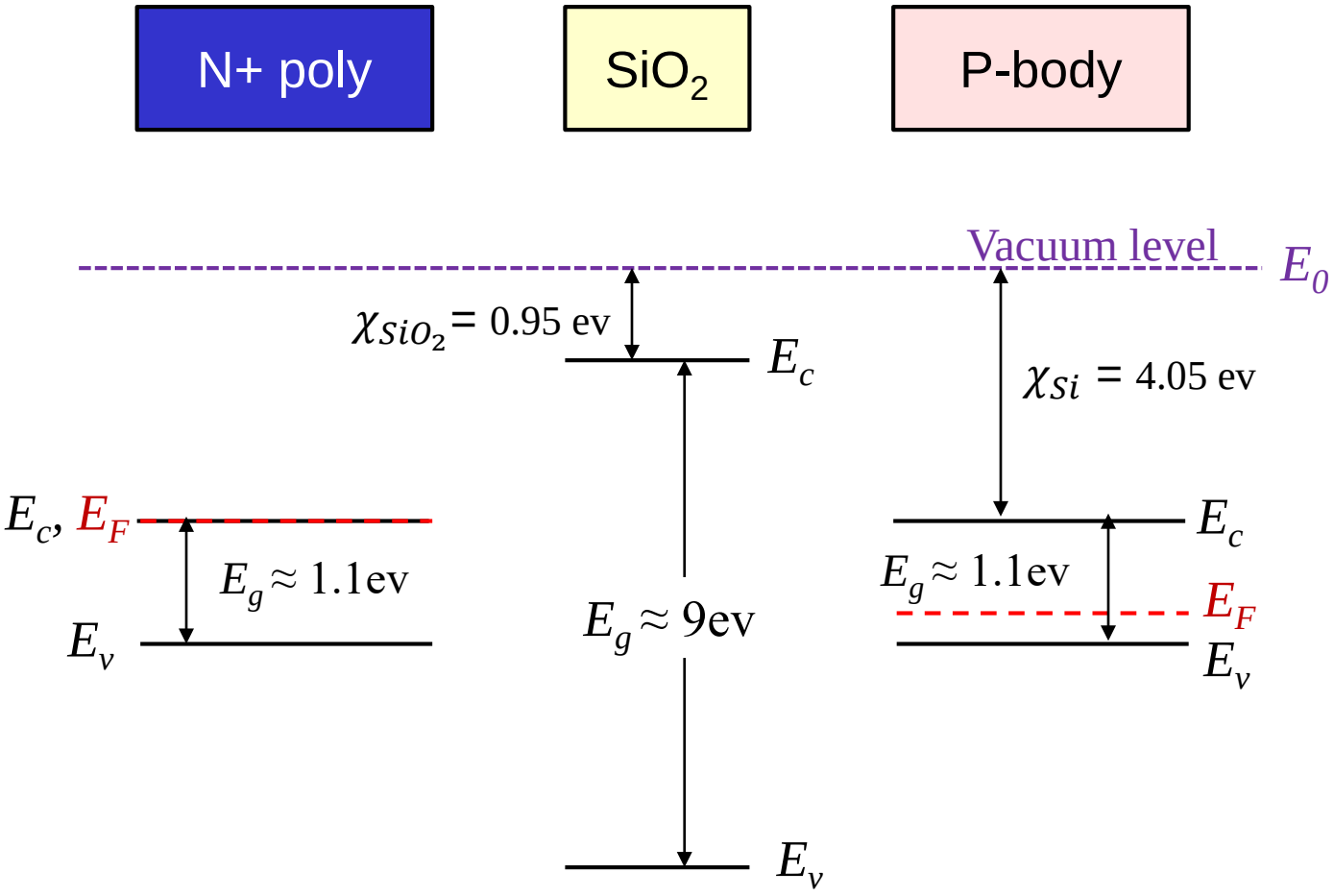


MOS transistor

- Gate oxide film can be as thin as 1.5nm
- After 1970, gate usually made from heavily doped polysilicon
- Trend today is to return to metal gates

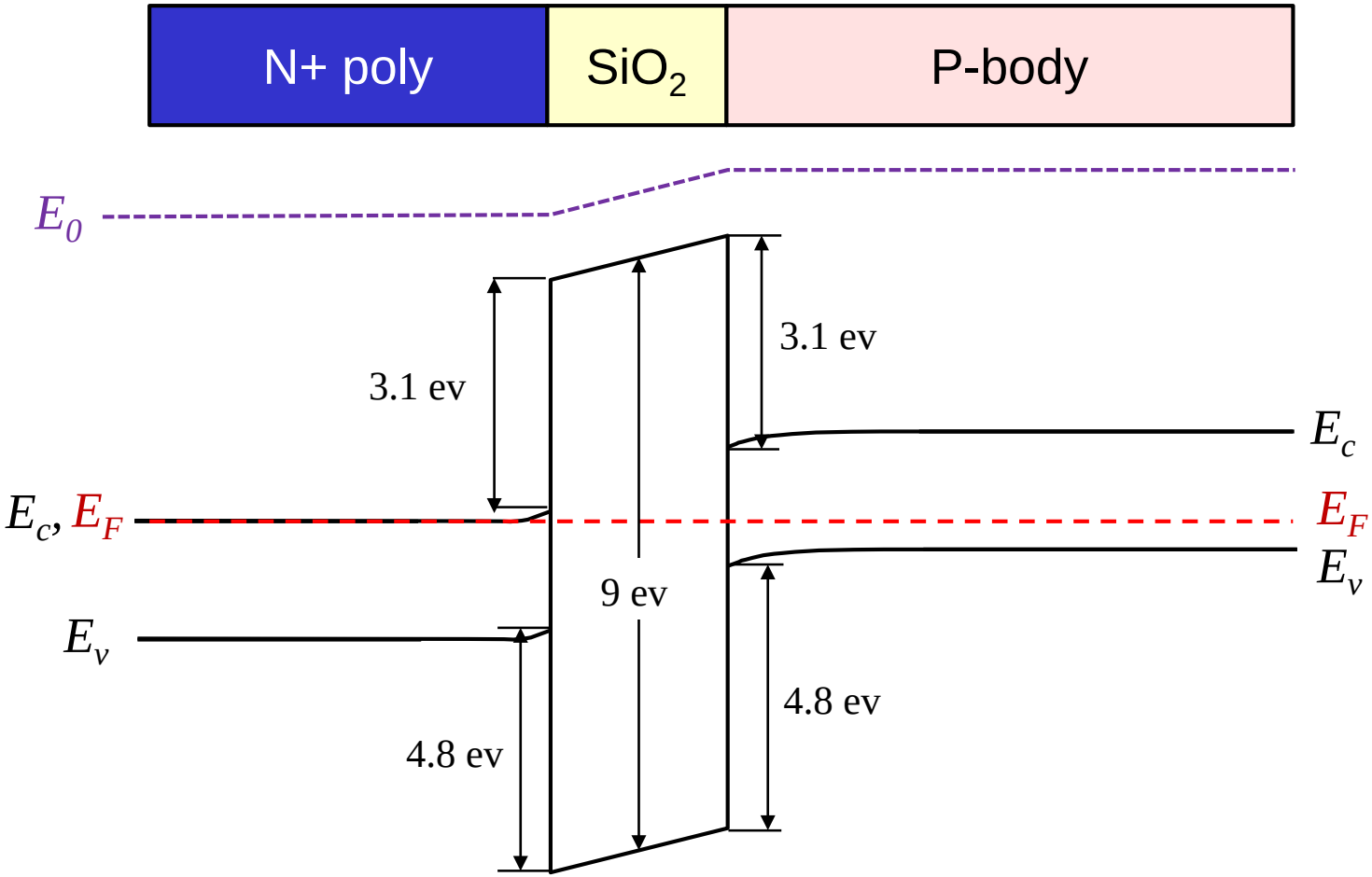
MOS Capacitor - Energy Band Diagram

- Three different materials:



MOS Capacitor – Thermal Equilibrium (V_g=0)

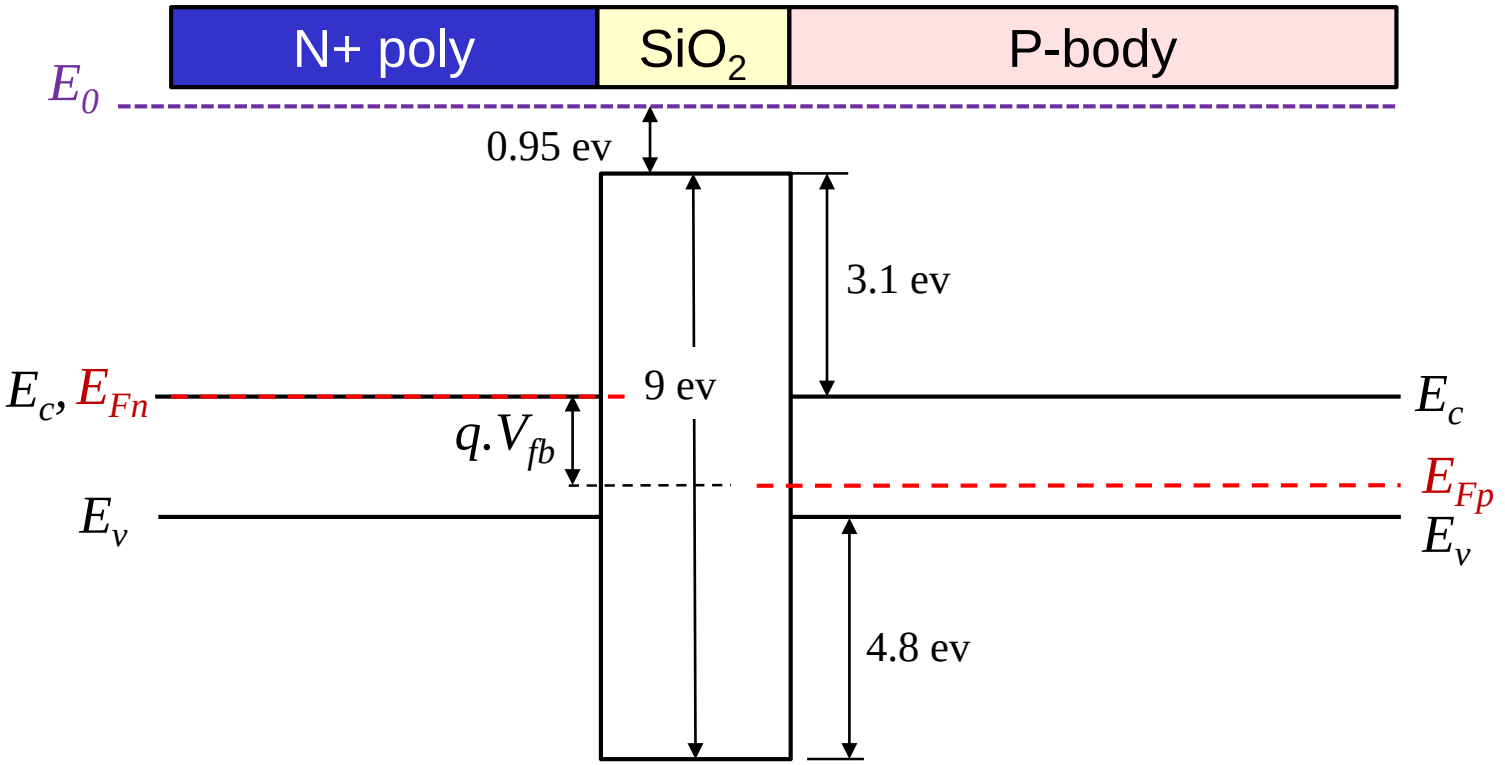
- What happens when we bring these materials together?



- Potential difference between N^+ gate and P body at zero bias
  - analogous to built-in voltage of PN junction

Flat Band Condition

- Necessary to apply small negative voltage V_{fb} on gate to make energy bands flat at oxide surface



- Flat-band voltage V_{fb} is equal to difference in Quasi-Fermi levels between two terminals under flat-band conditions
- For heavily doped N+ gate:

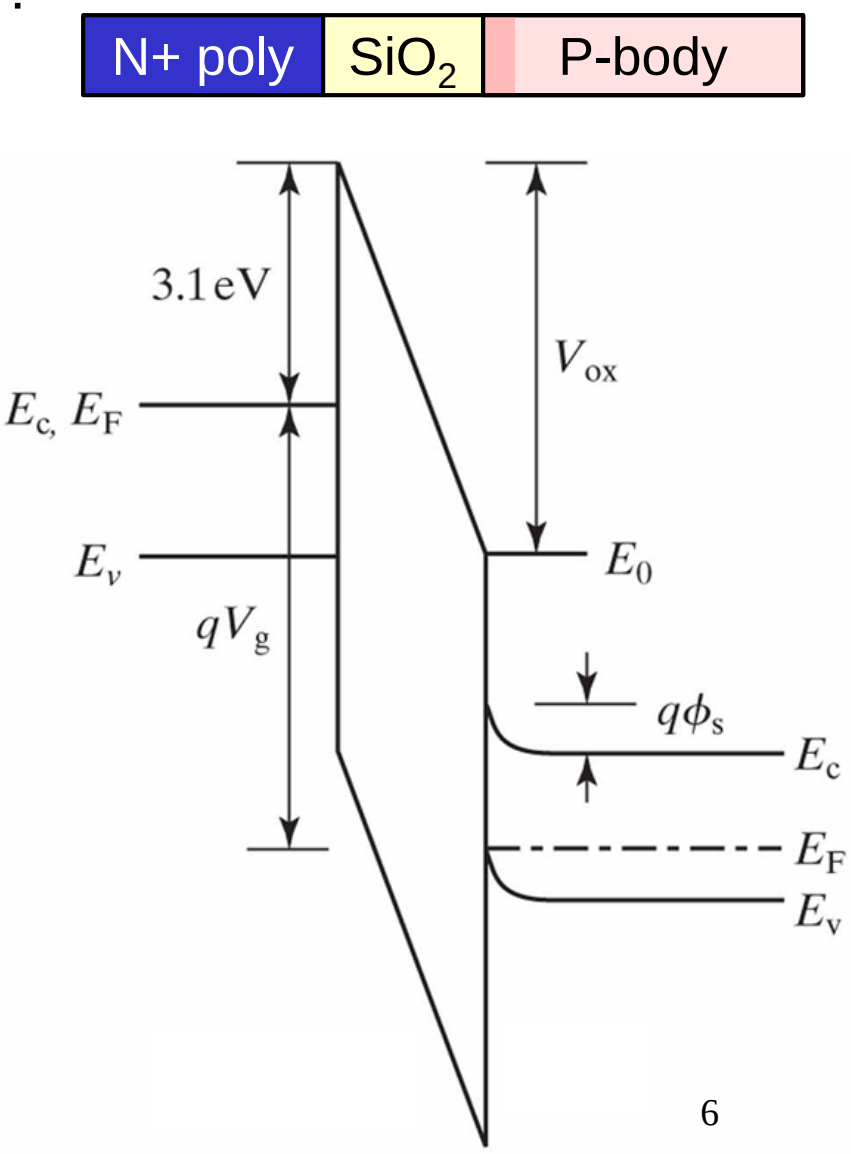
$$V_{fb} \approx \left(E_{Fp} - E_c\right)/q = \left(E_{Fp} - E_v - E_g\right)/q$$

Surface Accumulation

- What happens if we take $V_g < V_{fb}$?
- Band diagram on gate side pushed upward
- E_c on body side bends up towards oxide surface
- Surface potential $\emptyset_s$ is a measure of amount of band bending
  - note that $\emptyset_s$ is negative if band bend upwards
- V_{ox} is potential across the oxide
  - also negative in accumulation
- V_g is the potential of gate relative to the body

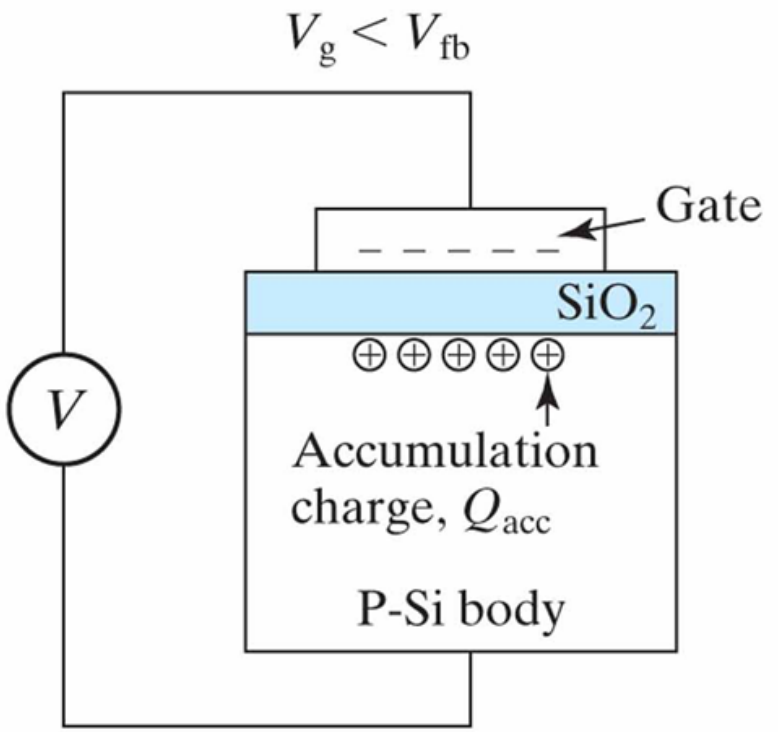
$$V_g = V_{fb} + \emptyset_s + V_{ox}$$

  - In flat-band, $\emptyset_s = V_{ox} = 0$



Charge Accumulation

- Negative voltage on gate attracts majority holes to surface
- Because E_v is closer to E_F at surface (compared to bulk), surface concentration is higher then p_0



$$p_s = N_a . e^{-q\emptyset_s/kT}$$

$$\emptyset_s = -\frac{kT}{q} . ln\left(\frac{p_s}{N_a}\right)$$

$$\text{If } \emptyset_s = -100\, mv, p_s \approx 50 \times N_a$$
$$\text{If } \emptyset_s = -200\, mv, p_s \approx 2200 \times N_a$$

- In accumulation, $\emptyset_s$ is small and can be ignored in a first order model which gives:

$$V_{ox} = V_g - V_{fb}$$

Accumulation Capacitance

- Gauss's Law: $\vec{E}_{ox} = -\frac{Q_{acc}}{\varepsilon_{ox}}$

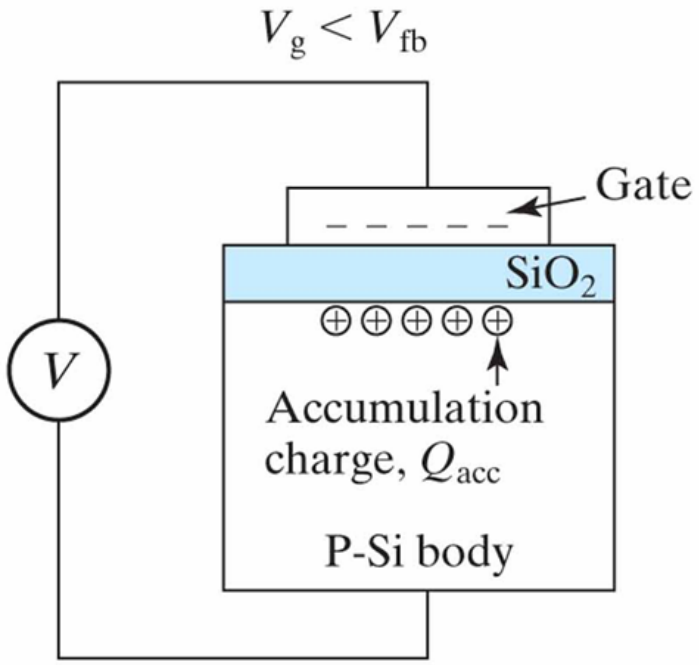
$$V_{ox} = \vec{E}_{ox}.T_{ox} = -\frac{Q_{acc}.T_{ox}}{\varepsilon_{ox}} = -\frac{Q_{acc}}{C_{ox}}$$

$$Q_{acc} = -C_{ox}(V_g - V_{fb})$$

- MOS capacitor in accumulation behaves like regular capacitor with $(Q = -C.V)$ but with a shift in V by V_{fb}
  - negative sign because voltage is measured at gate while charge is measured on body
- More generally:

$$V_{ox} = -\frac{Q_{bod}}{C_{ox}}$$

where Q_{bod} is total charge in body (including Q_{acc})



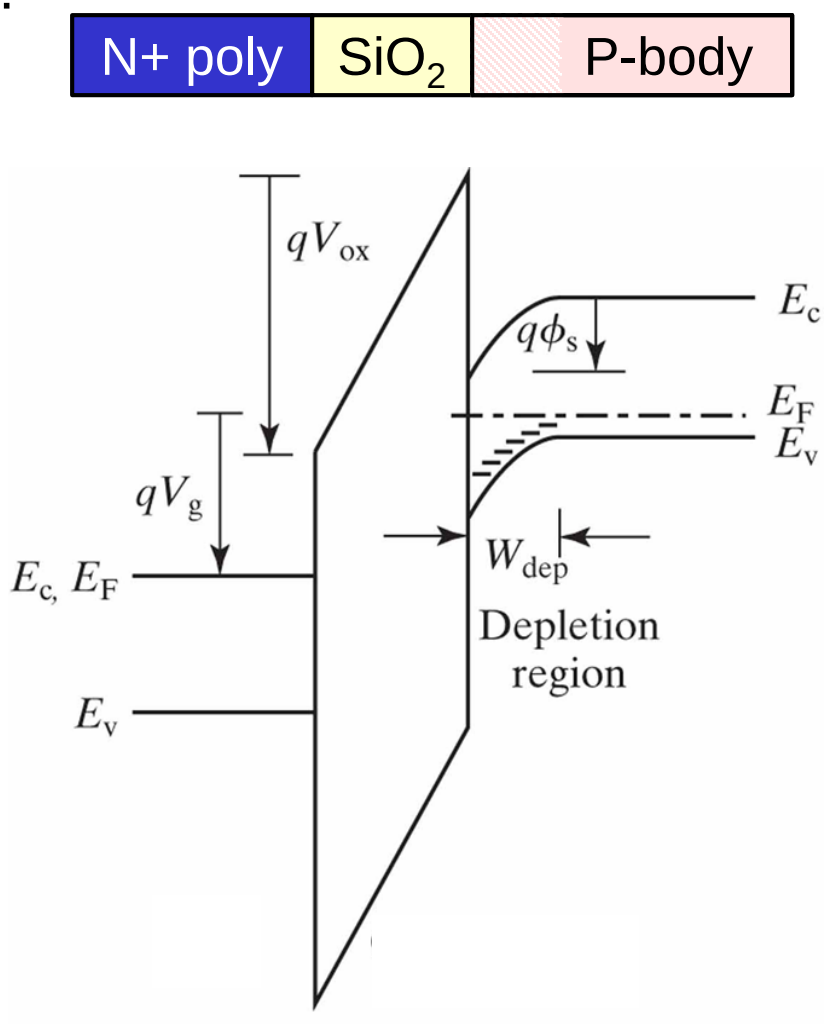
Q_{acc} is accumulated charge per unit area (C/cm^2)

T_{ox} is oxide thickness (cm)

C_{ox} is oxide capacitance per unit area (F/cm^2)

Surface Depletion

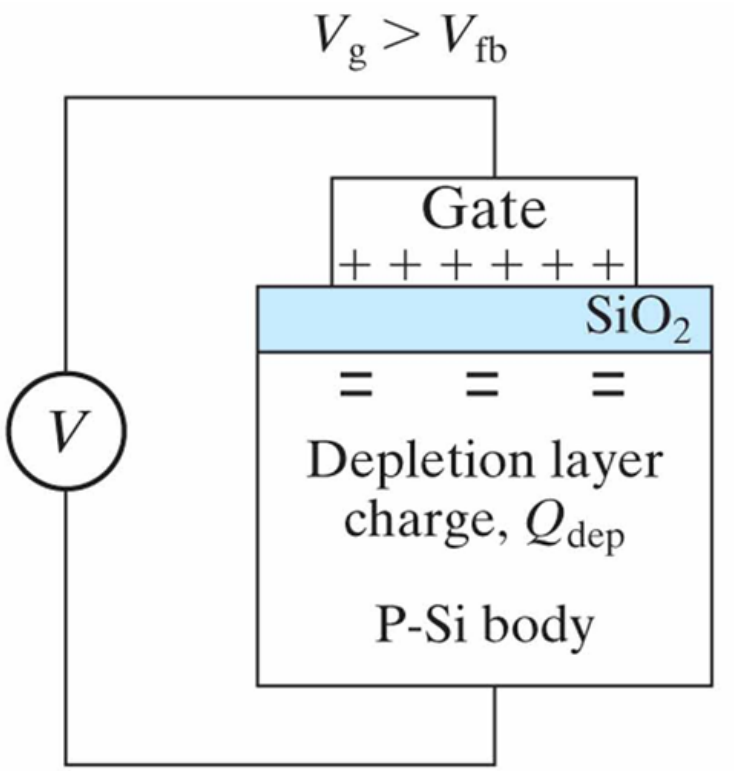
- What happens if we take $V_g > V_{fb}$?
- Band diagram on gate side pulled downward
- E_c on body side bends down towards oxide surface
- More positive voltage on gate repels majority holes from surface
- Because E_F is now far from E_c and E_v at surface, electron and hole densities are both small.
- There is now a depletion region at the surface with residual negative charge due to uncompensated acceptor ions



Depletion Width

$$V_{ox} = -\frac{Q_{bod}}{C_{ox}} = -\frac{Q_{dep}}{C_{ox}}$$

$$= \frac{q.N_a.W_{dep}}{C_{ox}}$$



- Using Poisson's eqn. as we did with reverse biased PN junction:

$$W_{dep} = \sqrt{(2\varepsilon_s.\emptyset_s)/q.N_a}$$

- which gives:

$$V_{ox} = \frac{\sqrt{2q.N_a.\varepsilon_s.\emptyset_s}}{C_{ox}} \quad \text{and} \quad \emptyset_s = \frac{q.N_a.W_{dep}^2}{2\varepsilon_s}$$

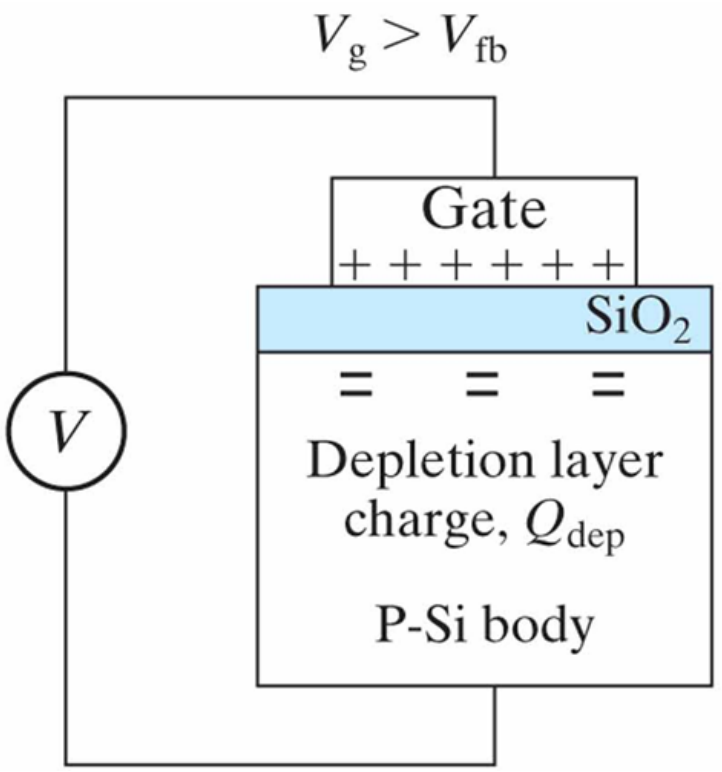
Charge Depletion

- As V_g increases, hole concentration at surface decreases as electron concentration at surface increases

$$p_s = N_a . e^{-q\emptyset_s/kT}$$

$$n_s = \frac{n_i^2}{N_a} . e^{+q\emptyset_s/kT}$$

- In depletion, $\emptyset_s$ is no longer negligible
  - can solve following quadratics to yield $\emptyset_s$ or W_{dep} as a function of V_g



$$V_g = V_{fb} + \emptyset_s + V_{ox} = V_{fb} + \emptyset_s + \frac{\sqrt{2q . N_a . \varepsilon_s . \emptyset_s}}{C_{ox}}$$

$$V_g = V_{fb} + \frac{q . N_a . W_{dep}^2}{2\varepsilon_s} + \frac{q . N_a . W_{dep}}{C_{ox}}$$

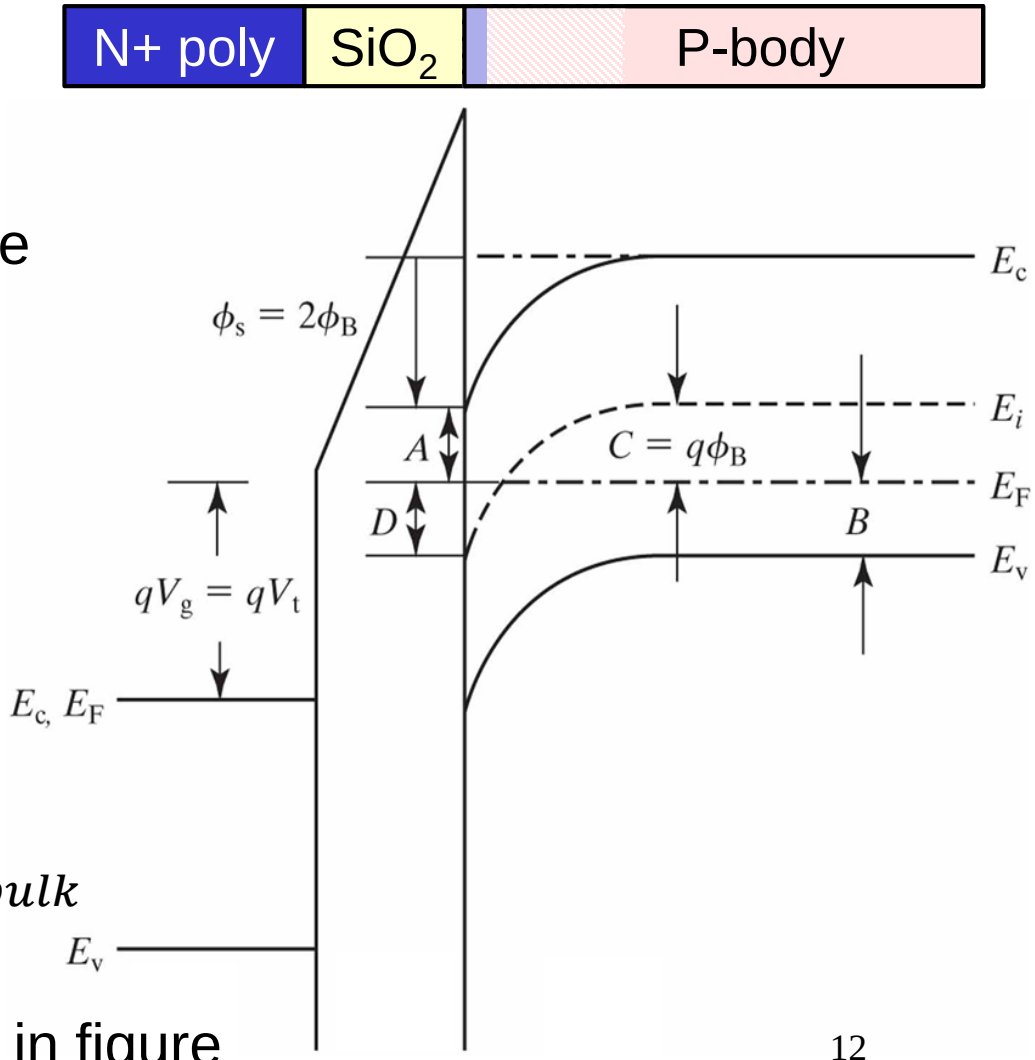
Surface Inversion

- What happens if we make V_g increasingly more positive?
- p_s continues to decrease
- n_s continues to increase
- At some point, surface changes from P-type to N-type – this is called inversion
- Threshold of inversion is defined as that condition in which surface electron concentration becomes equal to bulk hole concentration

$$n_s = N_a$$

$$(E_c - E_F)_{surface} = (E_F - E_v)_{bulk}$$

i.e., $A = B$ which implies $C = D$ in figure



Threshold Condition

- Surface potential at threshold

$$\emptyset_{st} = (C + D)/q = 2C/q$$

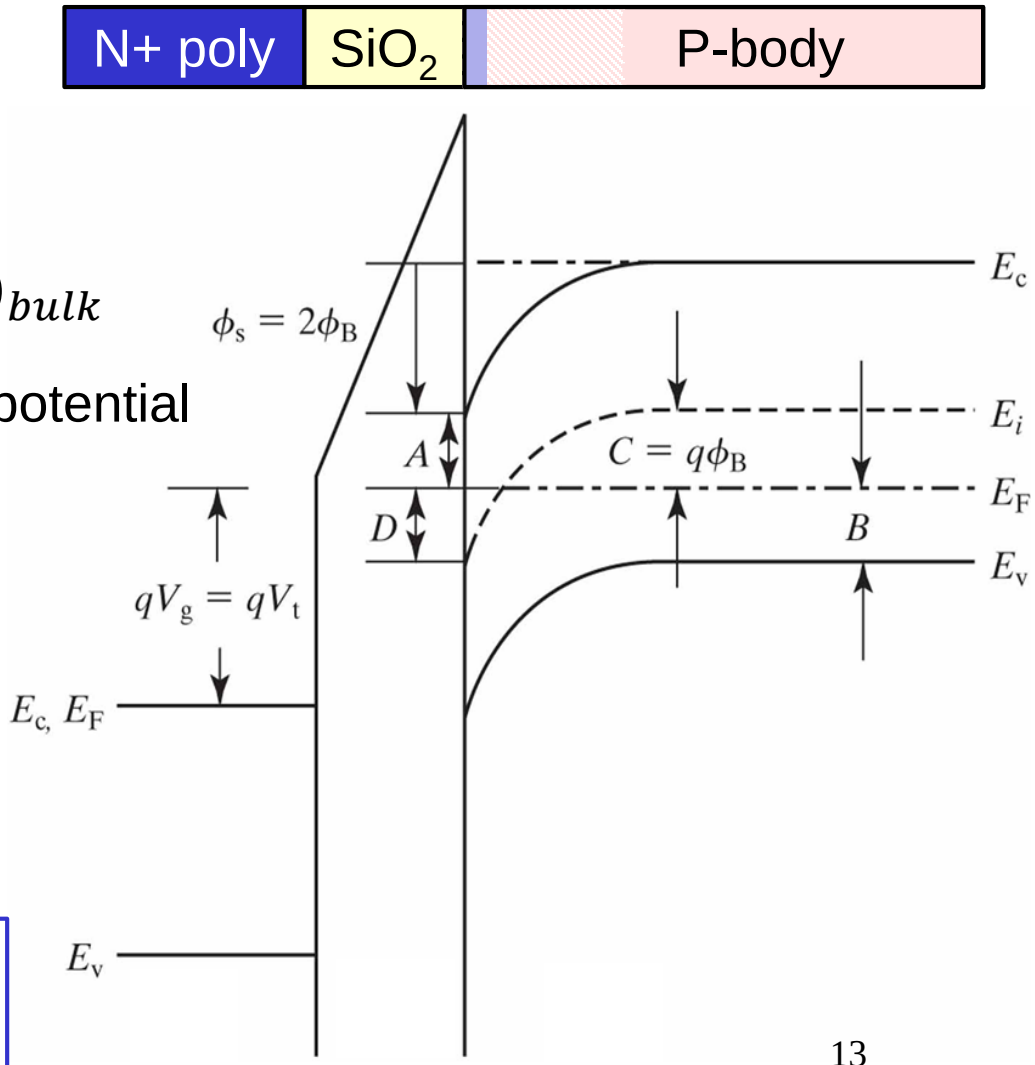
$$= 2\emptyset_B$$

- where $q.\emptyset_B \equiv \frac{E_g}{2} - (E_F - E_v)_{bulk}$
  - $\emptyset_B$ is sometimes called bulk potential
- Assuming $N_c \approx N_v$,

$$q.\emptyset_B = kT.ln\frac{N_v}{n_i} - kT.ln\frac{N_v}{N_a}$$

so, $\emptyset_B = \frac{kT}{q}.ln\frac{N_a}{n_i}$

$$\emptyset_{st} = 2\emptyset_B = 2.\frac{kT}{q}.\ln\frac{N_a}{n_i}$$



Threshold Voltage

$$V_g = V_{fb} + \emptyset_s + V_{ox}$$

- Substituting:

$$V_{ox} = \frac{\sqrt{2q.N_a.\varepsilon_s.\emptyset_s}}{C_{ox}} \quad \text{and} \quad \emptyset_s = \emptyset_{st} = 2\emptyset_B$$

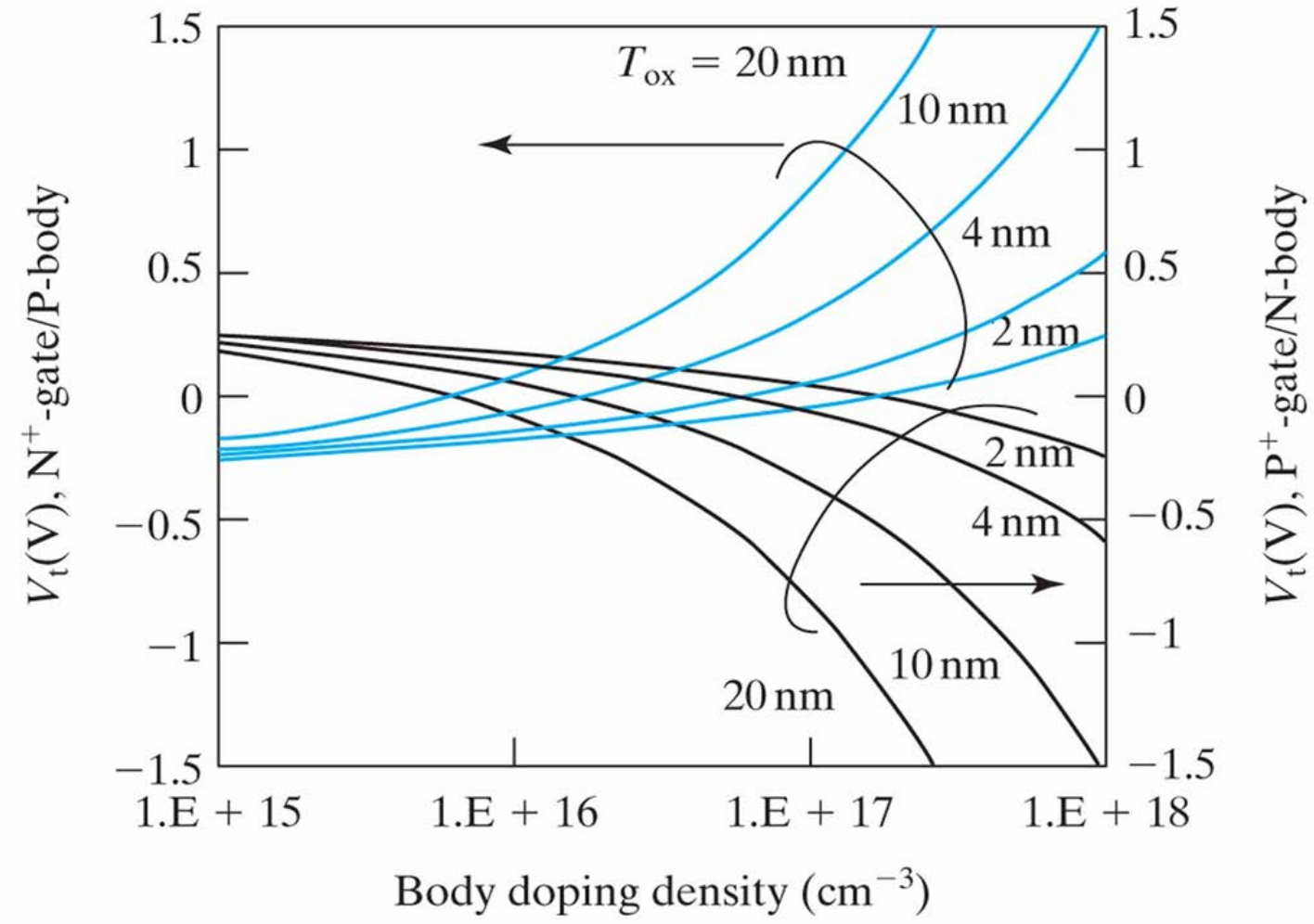
$$V_t = (V_g)_{\text{at threshold}} = V_{fb} + 2\emptyset_B + \frac{2.\sqrt{q.N_a.\varepsilon_s.\emptyset_B}}{C_{ox}}$$

- <u>For N-type body:</u>

$$V_t = V_{fb} - 2\emptyset_B - \frac{2.\sqrt{q.N_d.\varepsilon_s.\emptyset_B}}{C_{ox}} \quad \text{and} \quad \emptyset_{st} = -2\emptyset_B$$

$$\emptyset_B = \frac{kT}{q} ln \frac{N_d}{n_i} \qquad (note\ that\ \emptyset_B is\ always\ positive)$$

Threshold Voltage vs. Body Doping



$$V_t = V_{fb} \pm 2\emptyset_B \pm \frac{2.\sqrt{q.N_{body}.\varepsilon_s.\emptyset_B}}{C_{ox}}$$

+ for P-body
− for N-body

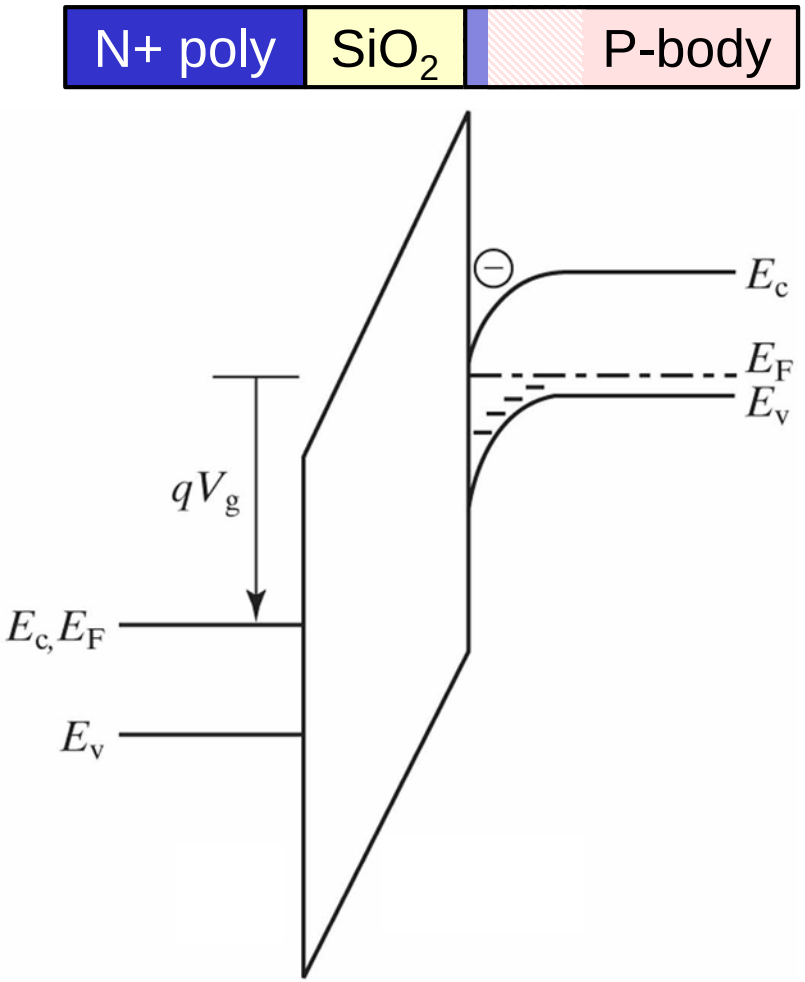
Strong Inversion

- If we increase V_g beyond V_t . . .
- There is now an inversion layer filled with inversion electrons
- Surface electron concentration increases dramatically with small increase in $\emptyset_s$

$$n_s = N_a . e^{q(\emptyset_s - 2\emptyset_B)/kT}$$

- Again, to a first order, $\emptyset_s$ does not increase significantly beyond $2\emptyset_B$
- Which implies depletion width has reached its maximum value

$$W_{dmax} = 2. \sqrt{\frac{\varepsilon_s . \emptyset_B}{q . N_a}}$$



Strong Inversion Charge

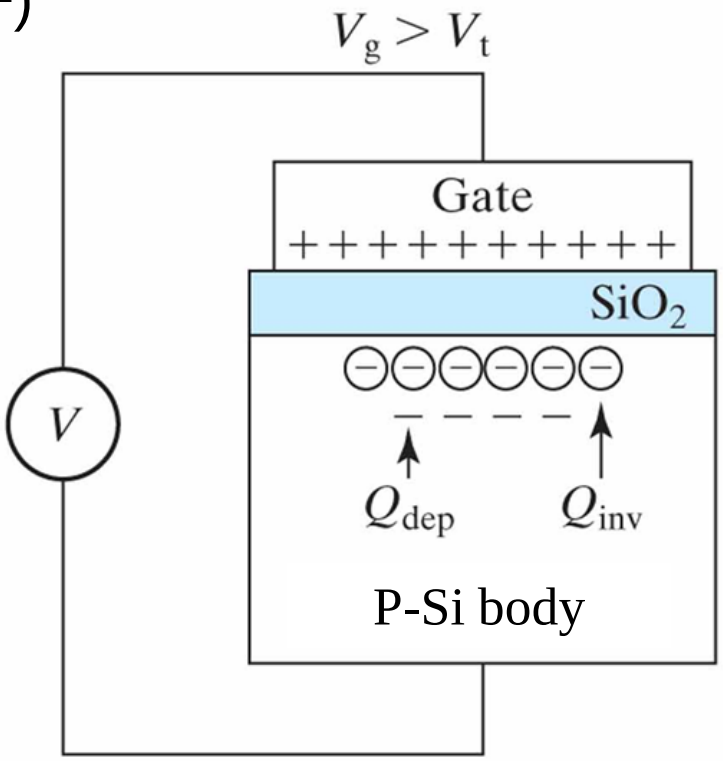
- Q_{inv} is inversion charge density (C/cm^2)

$$V_g = V_{fb} + \emptyset_s + V_{ox}$$

$$= V_{fb} + 2\emptyset_B - \frac{Q_{dep\_max}}{C_{ox}} - \frac{Q_{inv}}{C_{ox}}$$

$$= V_t - \frac{Q_{inv}}{C_{ox}}$$

- i.e., $\boxed{Q_{inv} = -C_{ox}(V_g - V_t)}$

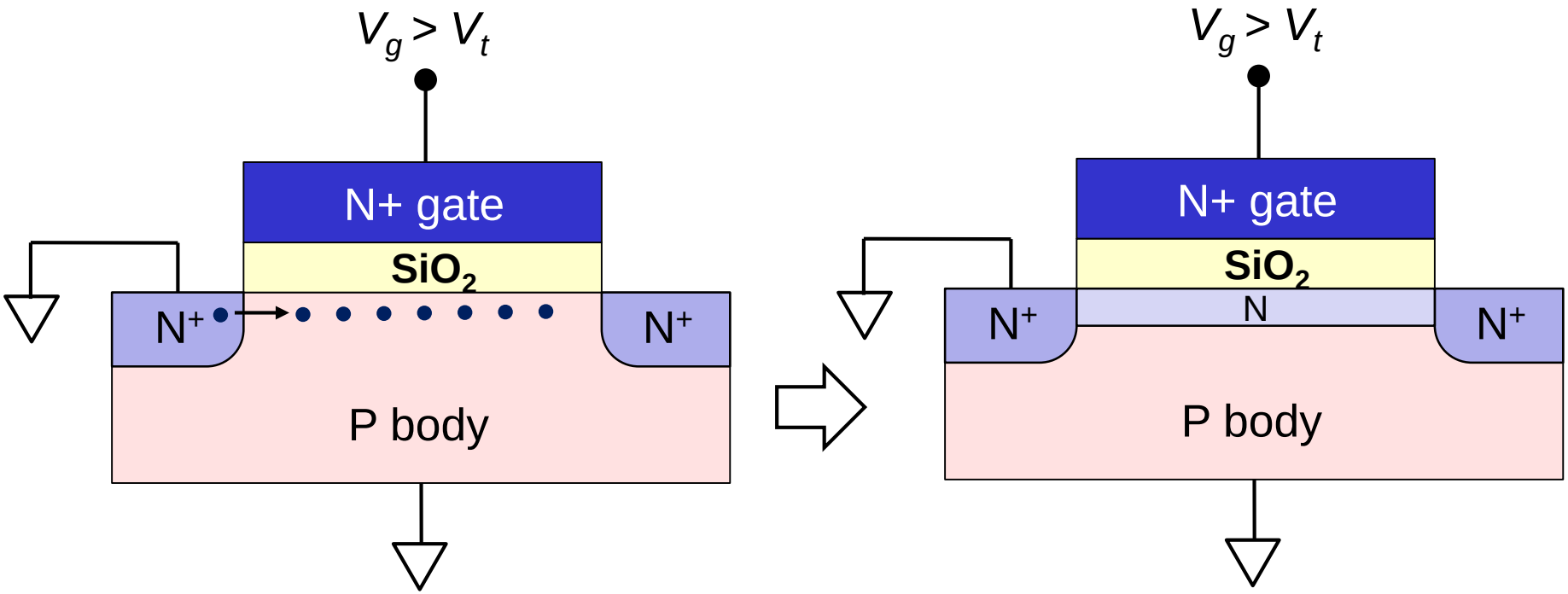


- MOS capacitor in strong inversion behaves as a capacitor with a voltage offset of V_t

Where do all these electrons come from?

MOS Transistor in Strong Inversion

- In MOS capacitor, inversion electrons generated thermally
  - can take many seconds in modern high quality silicon processes
- In MOS transistor, electrons rapidly supplied by N^+ source



Example: MOS Capacitor

- Consider an ideal MOS capacitor fabricated on a P-type silicon substrate with a doping of $5 \times 10^{16}\ cm^{-3}$ with an oxide thickness of $10nm$ and an N^+ poly gate. Determine:

a) Bulk potential $\emptyset_B$

b) Flat-band voltage V_{fb} of this capacitor

c) Oxide capacitance per unit area

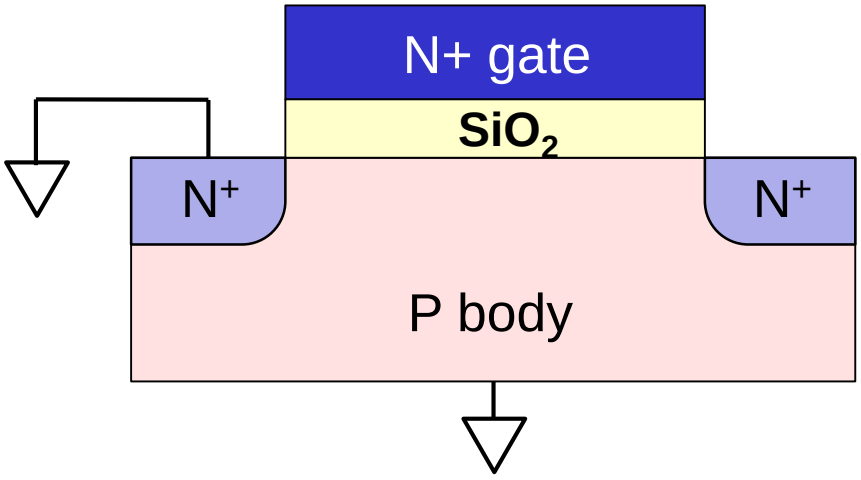
d) Threshold voltage V_t

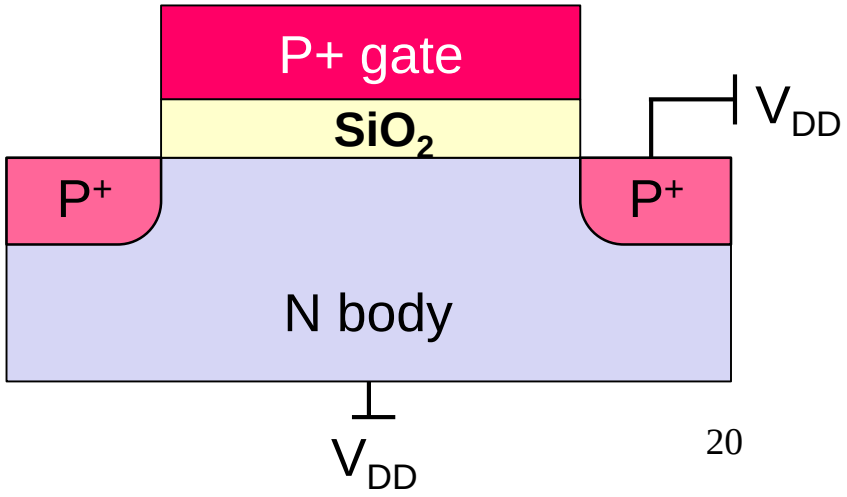
e) Maximum depletion width W_{dmax}

f) What would be the threshold if the poly gate were changed to heavy P^+ doping?

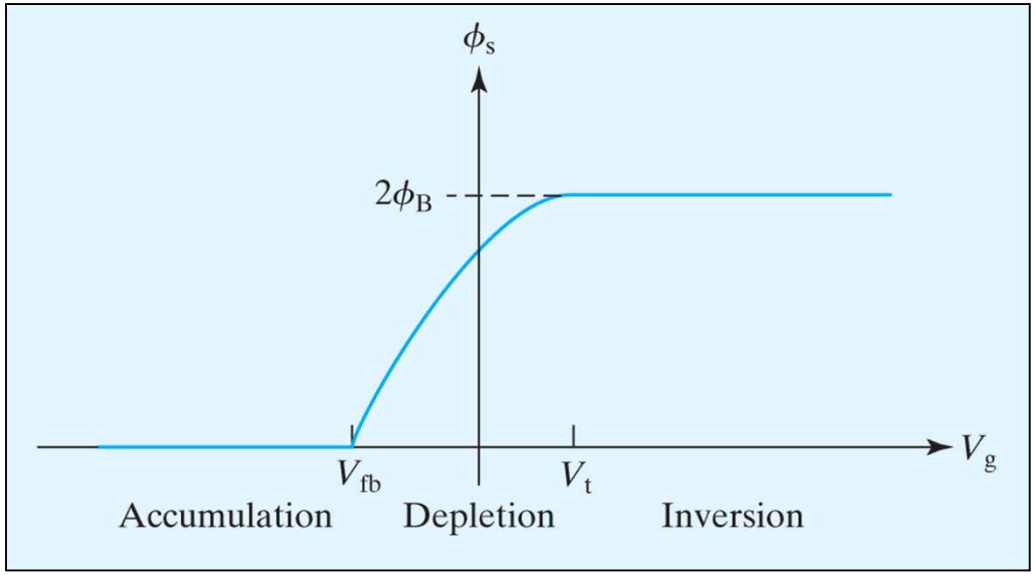
Gate Doping and Threshold Voltage

- P-body transistor normally operates in an IC with signal voltages that range from zero (ground) to some positive supply (V_{DD})
- V_t is normally set to a small positive voltage (e.g., 0.4V) so that the transistor does not have an inversion layer at $V_g = 0V$
  - A transistor that does not conduct at $V_{gs} = 0$ is known as an enhancement mode transistor
  - P^+ gate is not normally used with P-body device as it would raise threshold voltage too high (> 1V)
- N-body device is paired with P+ gate to give small negative V_t





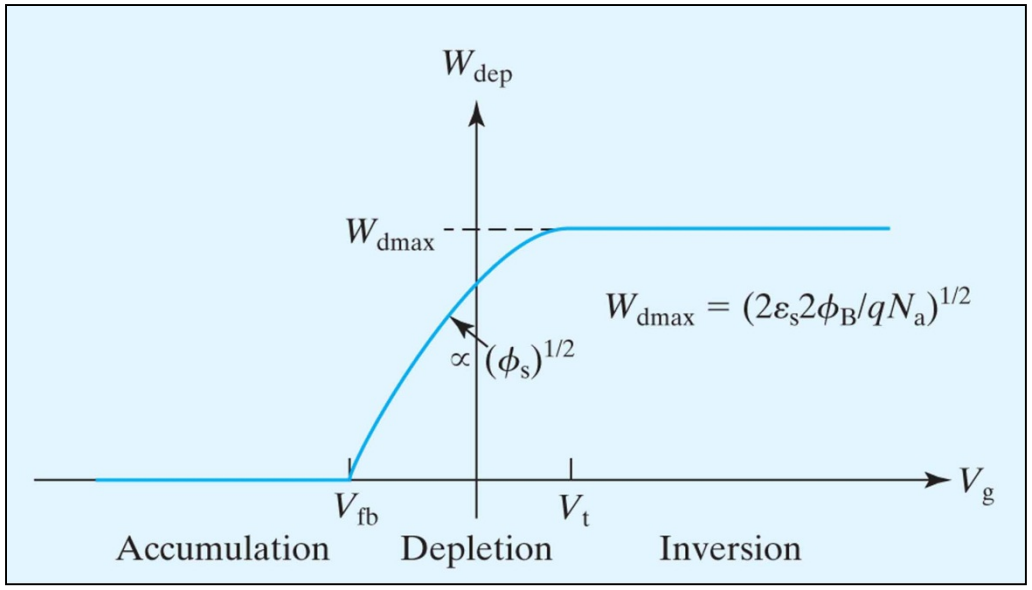
MOS Substrate Charge - Review



$\emptyset_s$ is zero at V_{fb} and near zero in accumulation region

As V_g increases above V_{fb}, $\emptyset_s$ increases until surface is inverted and $\emptyset_s = 2\emptyset_B$

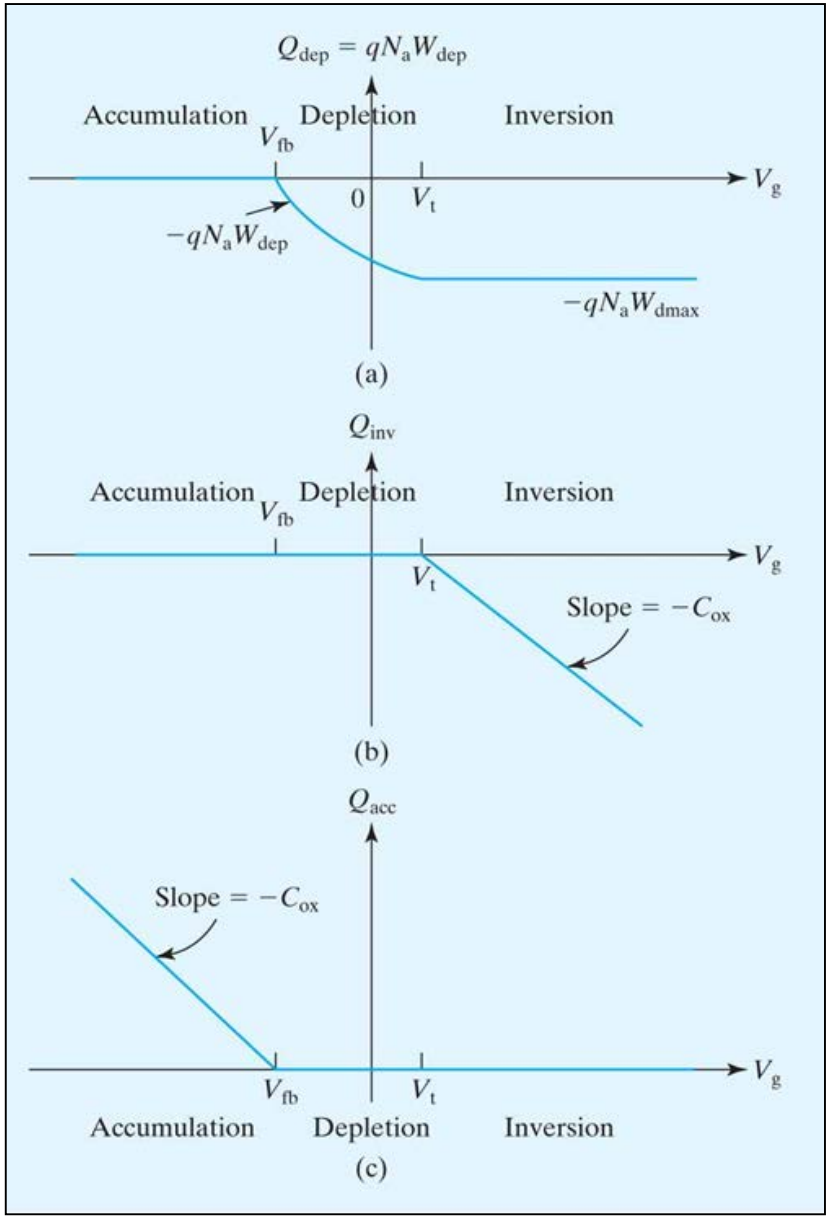
$\emptyset_s \approx 2\emptyset_B$ in inversion region



W_{dep} increases as the square root of the surface potential

At $V_g = V_t$, W_{dep} reaches its maximum value

Substrate Charge Components



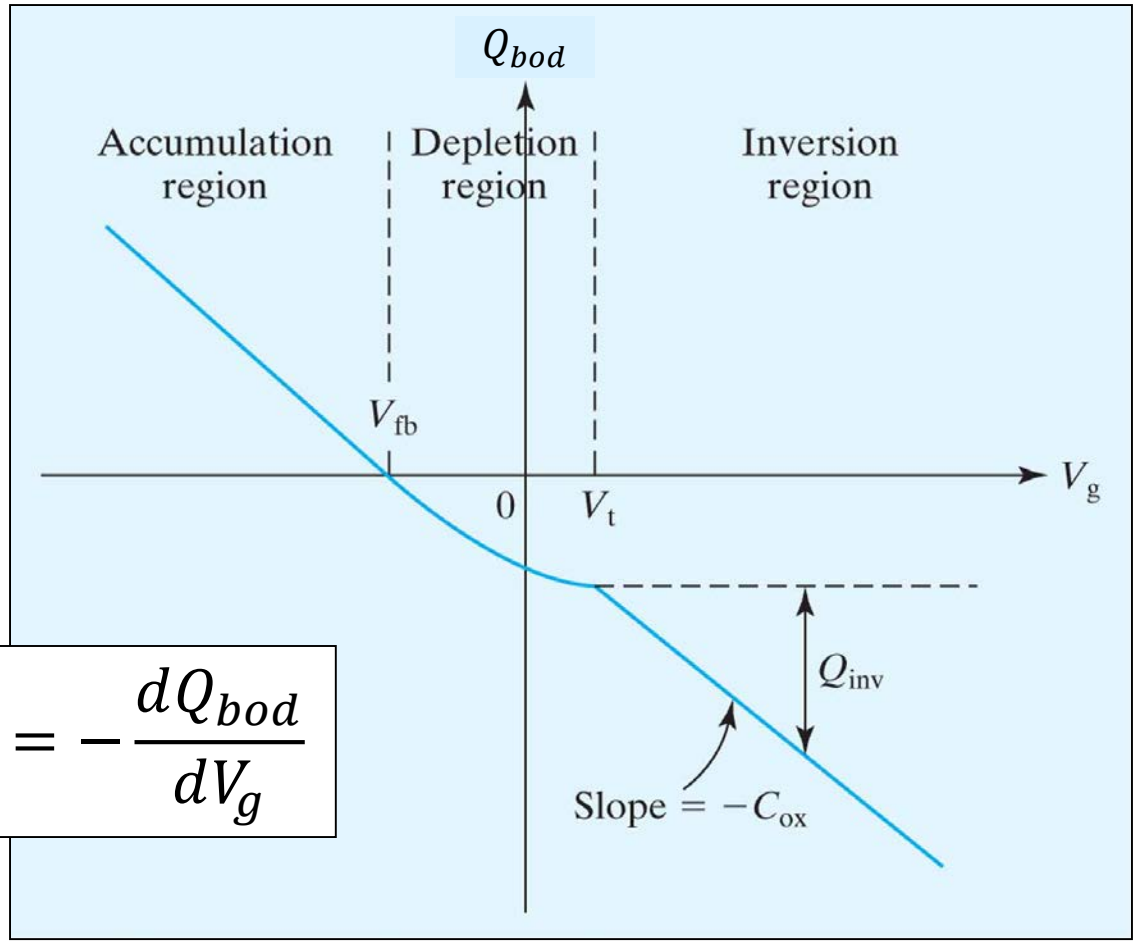
$$Q_{dep} = -q.N_a.W_{dep}$$

$$Q_{inv} = -C_{ox}(V_g - V_t)$$

$$Q_{acc} = -C_{ox}(V_g - V_{fb})$$

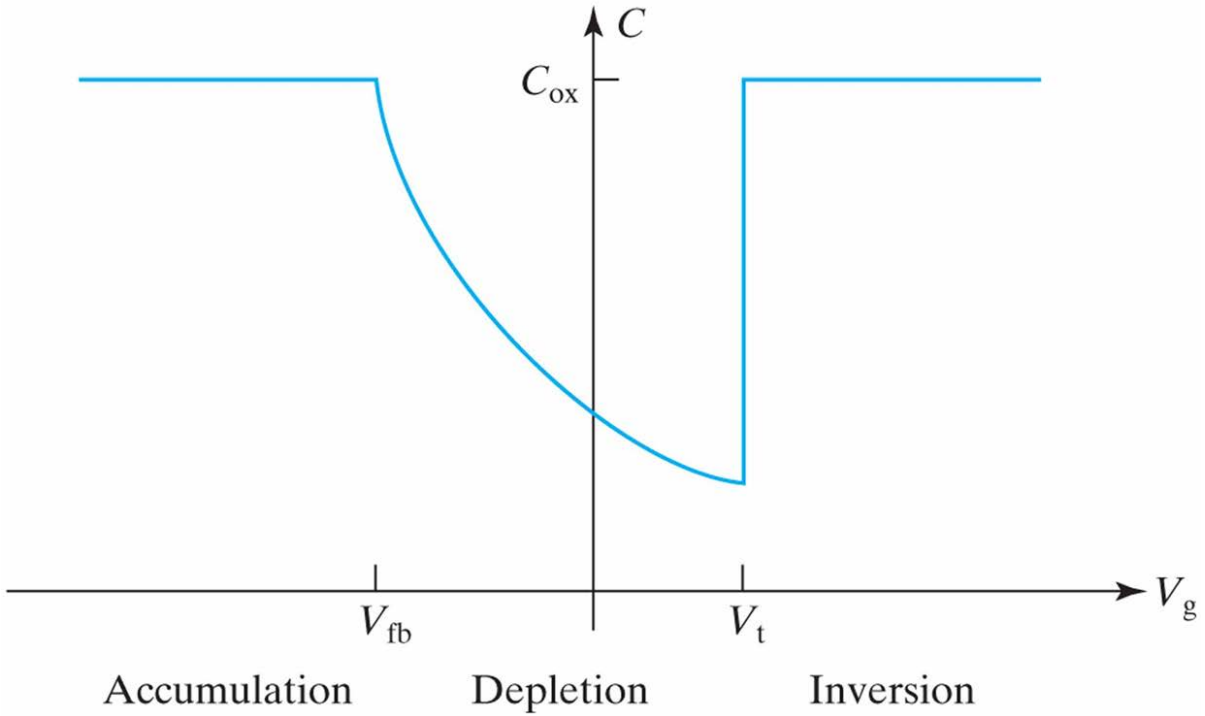
Total Substrate Charge

$$Q_{bod} = Q_{acc} + Q_{dep} + Q_{inv}$$

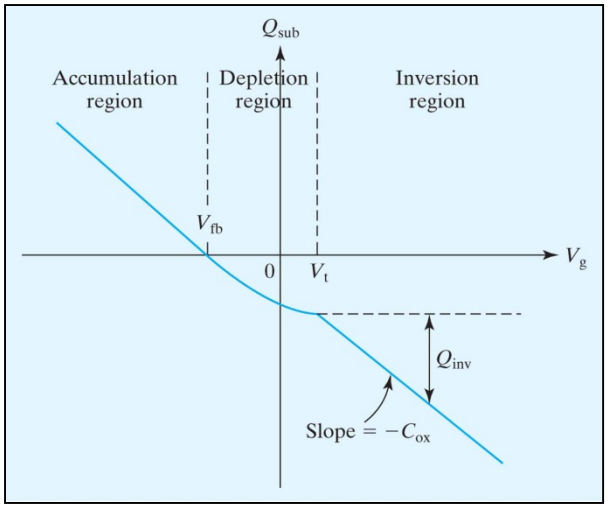


$$C \equiv \frac{dQ_g}{dV_g} = -\frac{dQ_{bod}}{dV_g}$$

MOS C-V Characteristics



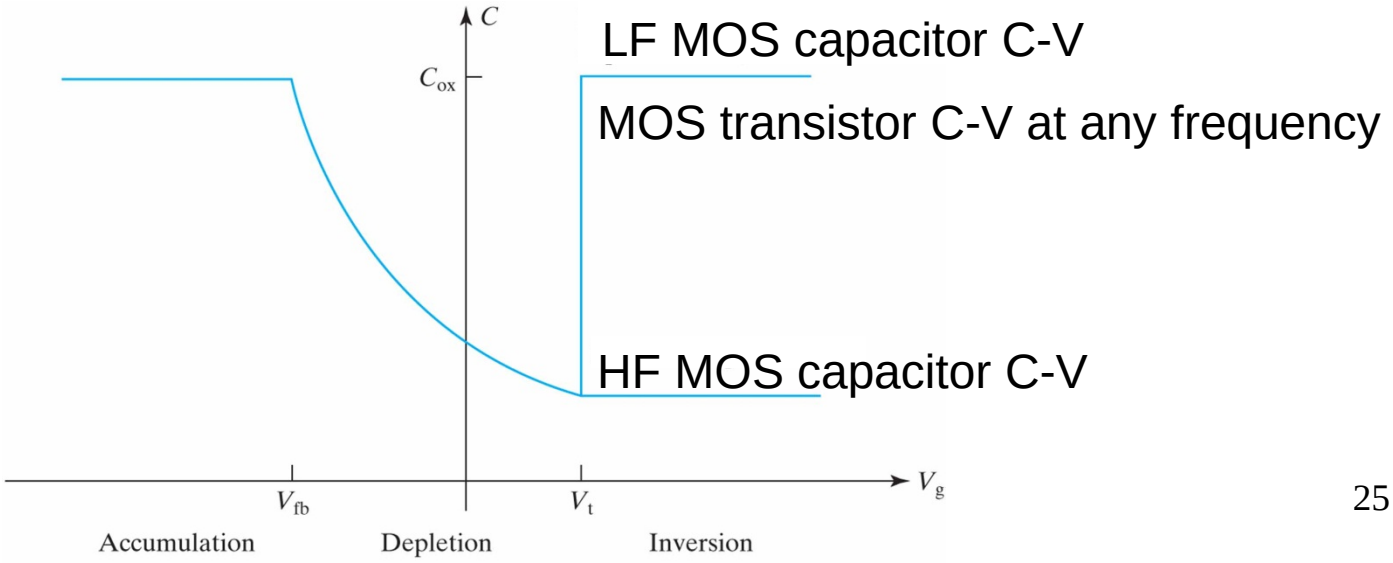
$$C \equiv \frac{dQ_g}{dV_g} = -\frac{dQ_{sub}}{dV_g}$$



- In depletion regime, C consists of two capacitors C_{ox} and C_{dep} in series: $\frac{1}{C} = \frac{1}{C_{ox}} + \frac{1}{C_{dep}}$ and $C_{dep} = \frac{\varepsilon_s}{W_{dep}}$
- Substituting for W_{dep}: $\frac{1}{C} = \sqrt{\frac{1}{C_{ox}^2} + \frac{2(V_g - V_{fb})}{q.N_a.\varepsilon_s}}$

MOS Capacitor C-V vs MOS Transistor C-V

- At high frequencies, MOS capacitor cannot (thermally) generate electrons fast enough to produce an inversion layer consistent with applied voltage V_g
  - so for $V_g > V_t$, C remains at maximum depletion value
  - In modern processes, high frequencies (in this context) may mean more than a few hertz!
- MOS Transistor has a good supply of electrons from nearby N^+ source region



Example: Capacitance Values

- A $10_{\mu m} \times 10_{\mu m}$ MOS capacitor is built with a N^+ poly gate on a P-type substrate with $N_a = 10^{17}\ cm^{-3}$ and a gate oxide thickness of $50\ nm$.

- What are the high and low frequency capacitances of the MOS capacitor when biased in strong inversion?

Second Order Effects

- So far, have ignored possibility of electric charge in oxide
  - fixed charge due to silicon ions at Si-SiO_2 interface
  - mobile charge due to impurities in oxide
  - sodium is a serious potential contaminant
- Oxide charge shifts flat-band voltage

$$V_{fb} \approx (E_F - E_c)/q - Q_{ox}/C_{ox}$$

- This, in turn, shifts threshold voltage
  - very serious in low voltage processes
- So far, have assumed accumulation and inversion layers to be zero width
  - Quantum solution of Poisson's eqn. at SiO_2 interface yields finite layer thickness ~ 5-15 Å
  - Effectively locates charge below interface by T_{inv}
  - Reduces C in accumulation and inversion domains
  - Reduces transistor performance with thin gate oxides (<10nm)

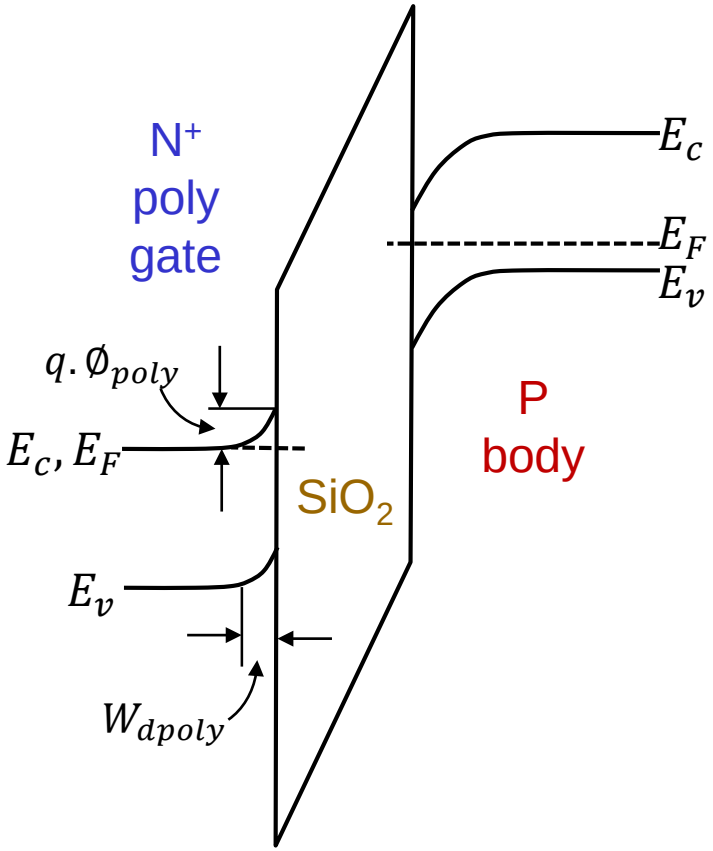
Polysilicon Gate Depletion

- So far, we have ignored any band bending in N^+ poly gate
  - poly is heavily doped but there will be small surface potential $\emptyset_{poly}$ <u>when body is biased into inversion</u>
- Creates a thin depletion layer in poly at SiO_2 interface
  - Gauss's Law gives:

$$W_{dpoly} = \varepsilon_{ox}.\vec{E}_{ox}/q.N_{poly}$$

  - W_{dpoly} may be 1-2 nm
  - Solving Poisson's Equation:

$$\emptyset_{poly} = \frac{-q.N_{poly}.W_{dpoly}^2}{2.\varepsilon_s}$$



- Summing potentials across interface:

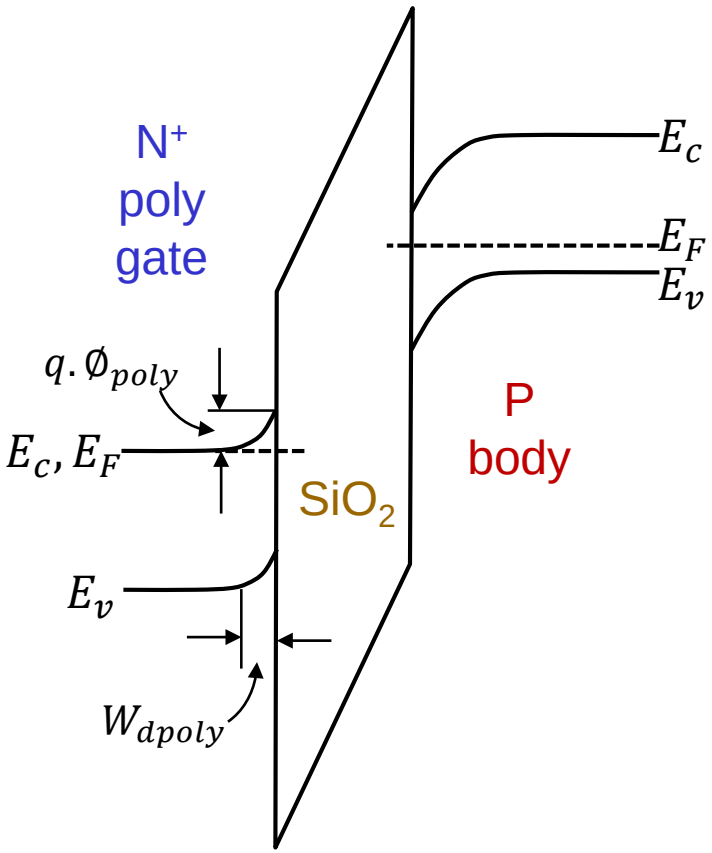
$$V_g = V_{fb} + \emptyset_{st} + V_{ox} - \emptyset_{poly}$$

Effects of Polysilicon Gate Depletion

- Gate Depletion decreases gate capacitance:

$$C = \left(\frac{1}{C_{ox}} + \frac{1}{C_{poly}}\right)^{-1} = \left(\frac{T_{ox}}{\varepsilon_{ox}} + \frac{W_{dpoly}}{\varepsilon_s}\right)^{-1}$$

$$= \frac{\varepsilon_{ox}}{T_{ox} + \left(W_{dpoly}/3\right)}$$



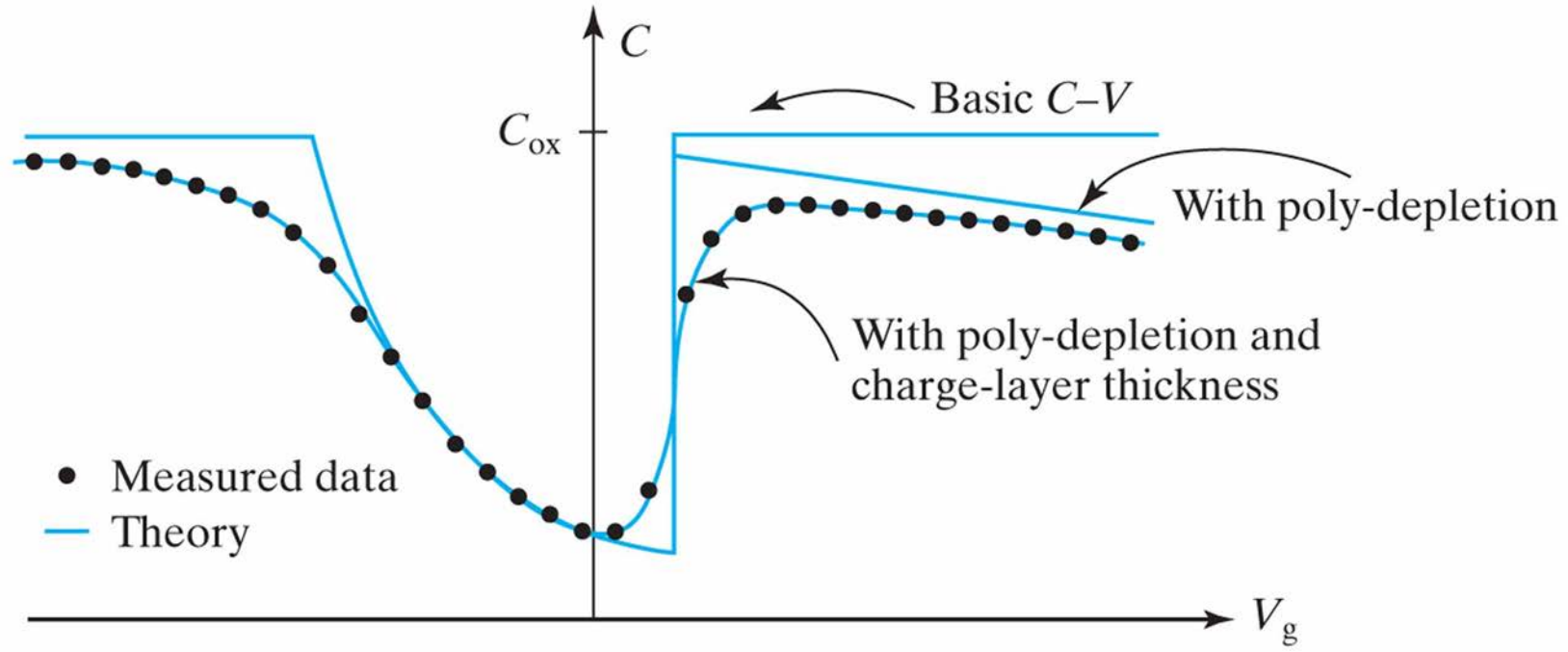
- Also, effectively reduces gate voltage:

$$Q_{inv} = -C_{ox}\left(V_g - \left|\emptyset_{poly}\right| - V_t\right)$$

Effective Oxide Capacitance

- Effective oxide thickness: $T_{oxe} = T_{ox} + W_{dpoly}/3 + T_{inv}/3$
- Effective oxide capacitance: $C_{oxe} = \varepsilon_{ox}/T_{oxe}$

$$Q_{inv} = -C_{oxe}(V_g - V_t)$$



- Poly depletion can be eliminated with metal gate

Example: Poly Gate Depletion

- Assume that V_{ox}, the voltage across a 2nm thin oxide is 1V. The N+ poly-gate doping is $N_{poly} = 8 \times 10^{19}\ cm^{-3}$ and substrate $N_a = 10^{17}\ cm^{-3}$. Assuming that channel is inverted, estimate:

a) W_{dpoly}

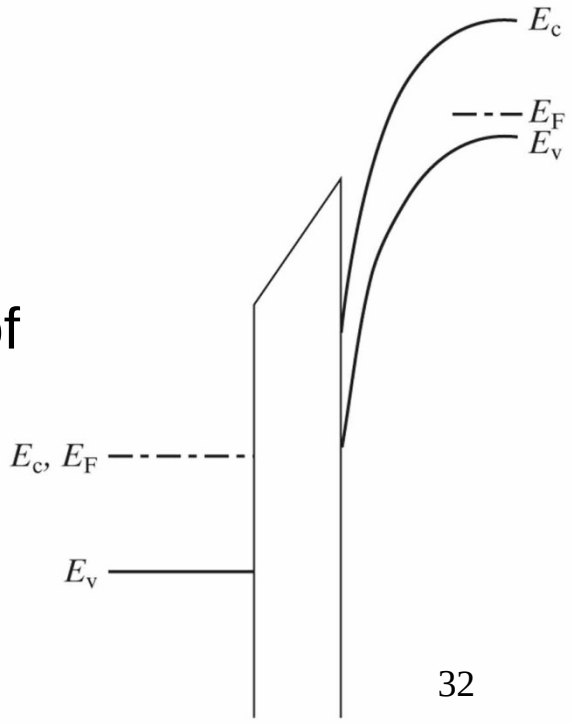
b) $\emptyset_{poly}$

c) V_g

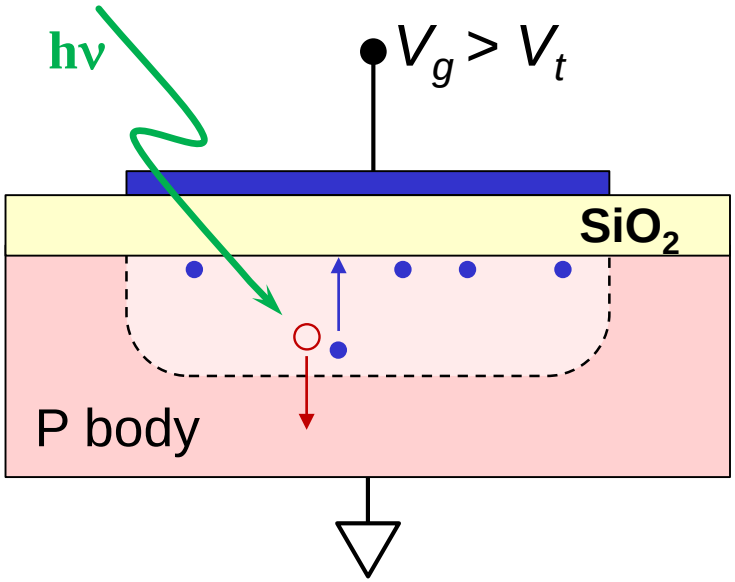
CCD Imager

- In CMOS imager, photodiode is used as photo-detector and CMOS circuitry is used to convert charge to voltage and amplify and transmit that voltage to output circuits
- In CCD imager, MOS capacitor is used both as a photo-detector and a charge transfer device to move photo-charge from pixel to output circuits

- Suppose a voltage $V_g > V_t$ is suddenly applied to gate of a MOS capacitor
- Thermal generation is slow – for a period of time there are no inversion electrons.
  - bands bend beyond $2\emptyset_B$
  - depletion region extends beyond W_{dmax}
- Known as deep depletion



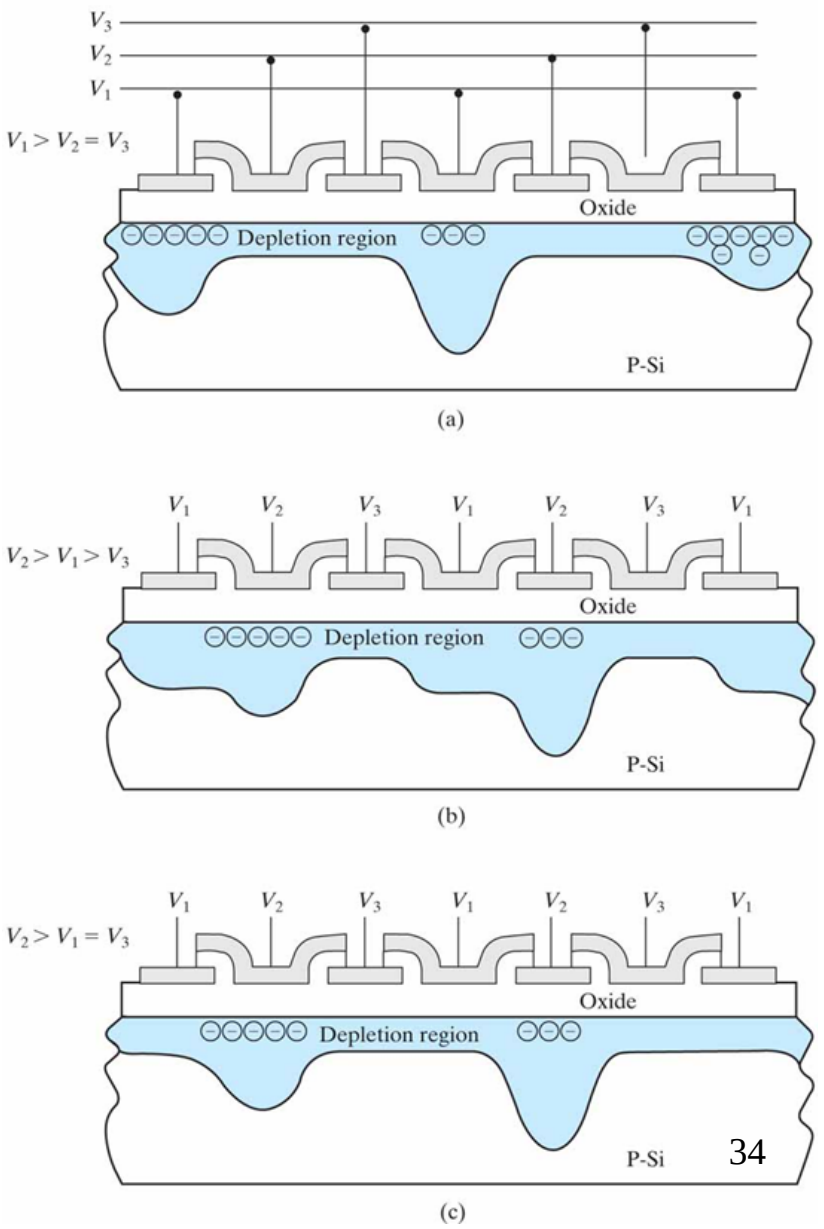
CCD Photodetector



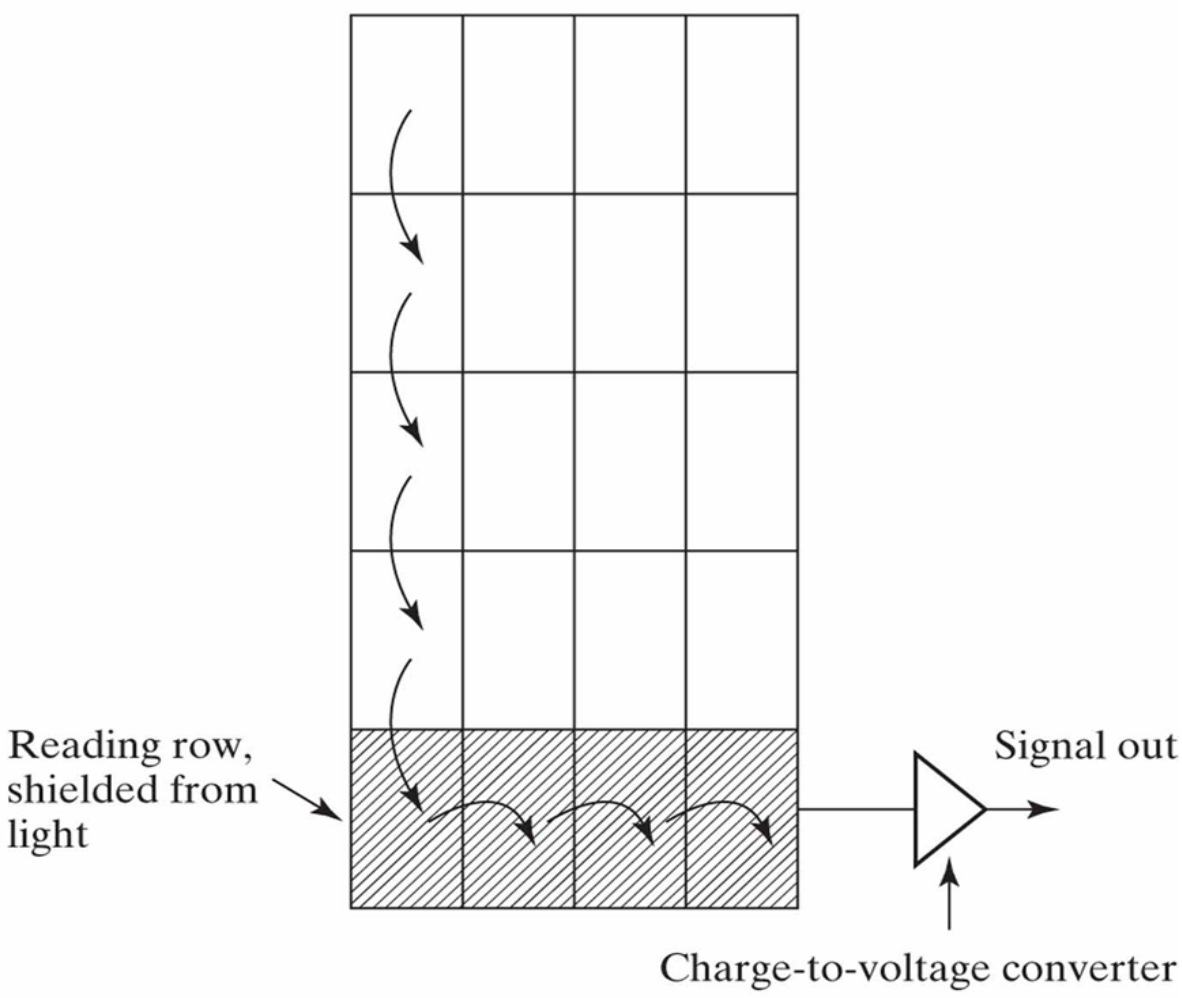
- If light shines on MOS capacitor in deep depletion, photons pass through thin poly gate and generate electron-hole pairs in depletion region
  - Photo-generated holes drift into substrate and are removed through substrate contact
  - Photo-generated electrons drift towards gate and are collected at oxide surface
- Number of electrons collected proportional to light intensity

CCD Charge Transport

- Once electrons are collected under a MOS gate, they can be passed along a row of adjacent gates with suitably timed multiphase clocks
- Every third gate functions as a photo-detector
- At end of exposure time, charges are passed along row toward output circuits
- Overlapping poly gates ensure high charge transfer efficiency



2-D CCD Imager



- 2-D array of charge packets are read row by row