EE 471: Transport Phenomena in Solid State Devices

Spring 2018

Lecture 8
MOS Transistor

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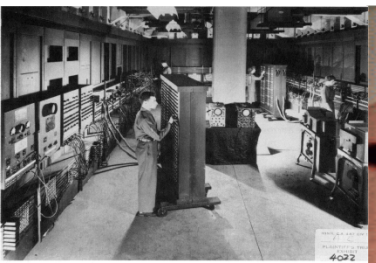
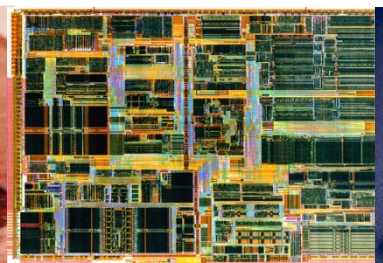
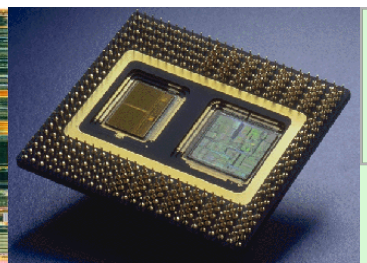
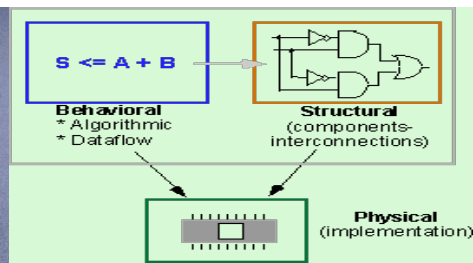
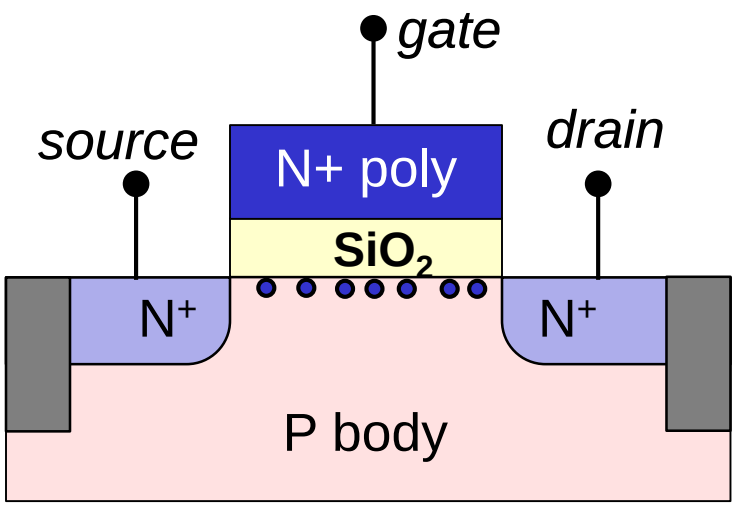
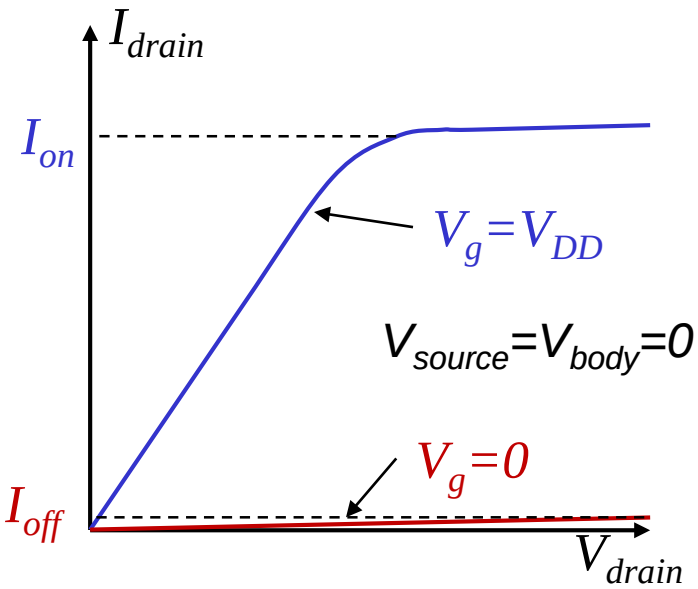
Adapted from Modern Semiconductor Devices for Integrated Circuits, Chenming Hu, 2010



MOSFET Transistor

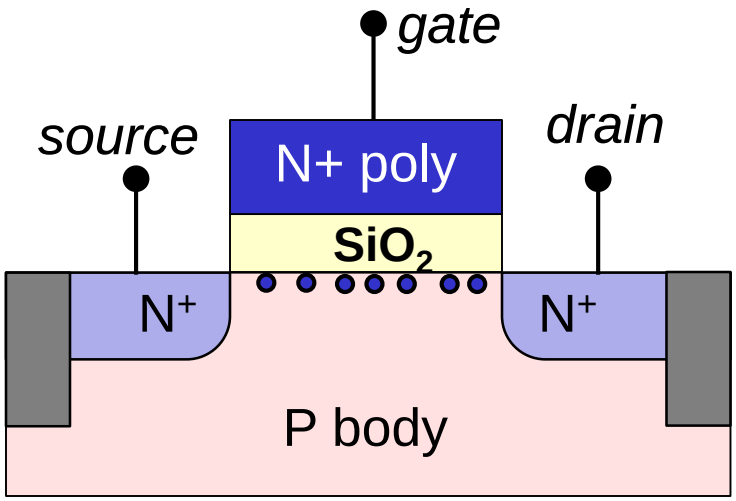


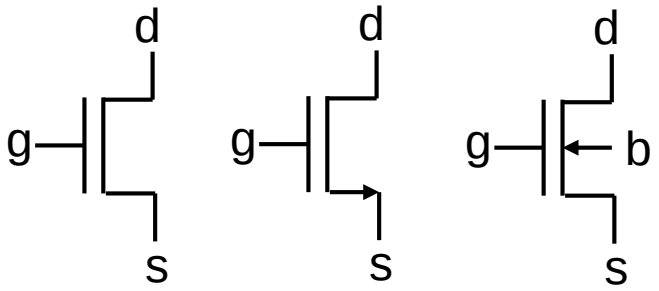


- Conduction between source and drain is controlled by gate voltage which induces and modulates inversion charge density
  - Inversion layer in a MOS transistor is often referred to as the channel
- MOS: Metal-Oxide-Semiconductor structure
- FET: Field Effect Transistor – conduction controlled by electric field

Complementary (CMOS) Technology

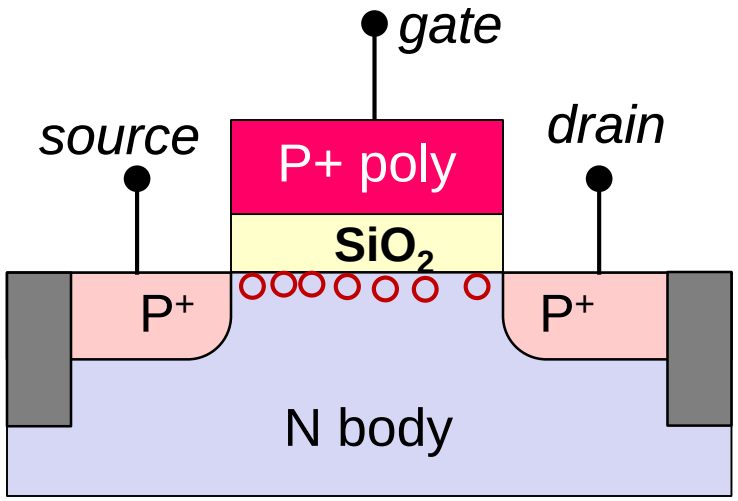
NFET or NMOS transistor

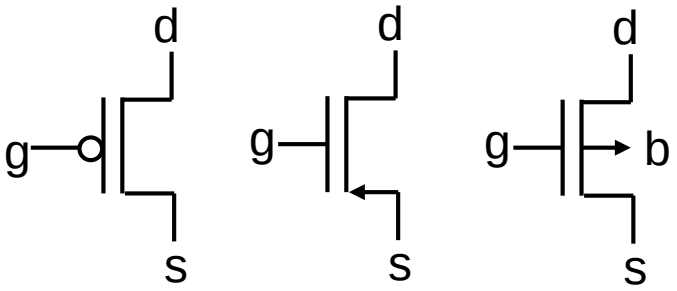




- P body normally connected to most negative voltage (0V, gnd)
- By definition: $V_s < V_d$

PFET or PMOS transistor





- N body normally connected to most positive voltage (V_{DD})
- By definition: $V_s > V_d$

Surface Mobility

- Current through the channel of an MOS transistor is a function of electron (or hole) mobility in the inversion region
  - in a MOS transistor, we care about mobility in inversion layer
  - i.e., mobility near boundary between Si and SiO_2
- Surface mobility (μ_{ns}, μ_{ps}) is not same as bulk mobility
  - surface mobility is reduced by surface roughness scattering
- Surface mobility is a function of $\vec{E}_{inv}$ average (vertical) electric field within the inversion charge layer
- For N^+ poly gate NFET: $$\vec{E}_{vert} \approx \frac{V_{gs} + V_t + 0.2V}{6.T_{oxe}}$$
- For P^+ poly gate PFET: $$\vec{E}_{vert} \approx -\frac{V_{gs} + 1.5V_t - 0.25V}{6.T_{oxe}}$$

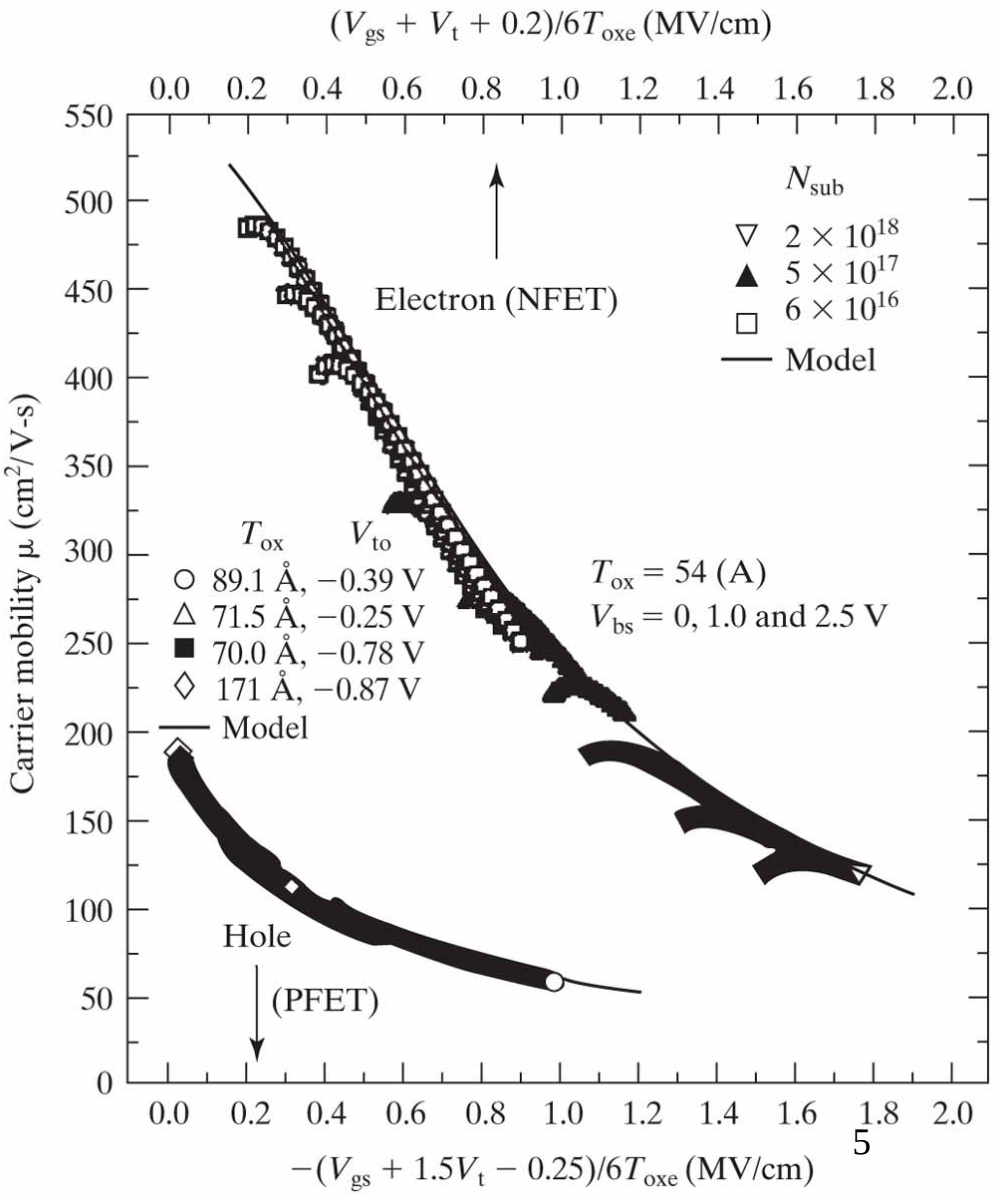
Empirical Mobility

- Empirically:

$$\mu_{ns} = \frac{540\ cm^2/V.s}{1 + \left(\frac{V_{gs} + V_t + 0.2V}{5.4 \times 10^6 . T_{oxe}}\right)^{1.85}}$$

$$\mu_{ps} = \frac{185\ cm^2/V.s}{1 - \left(\frac{V_{gs} + 1.5V_t - 0.25V}{5.4 \times 10^6\ . T_{oxe}}\right)}$$

- Surface roughness scattering is greater at higher V_g, higher V_t and thinner T_{oxe}



Example: Surface Mobility

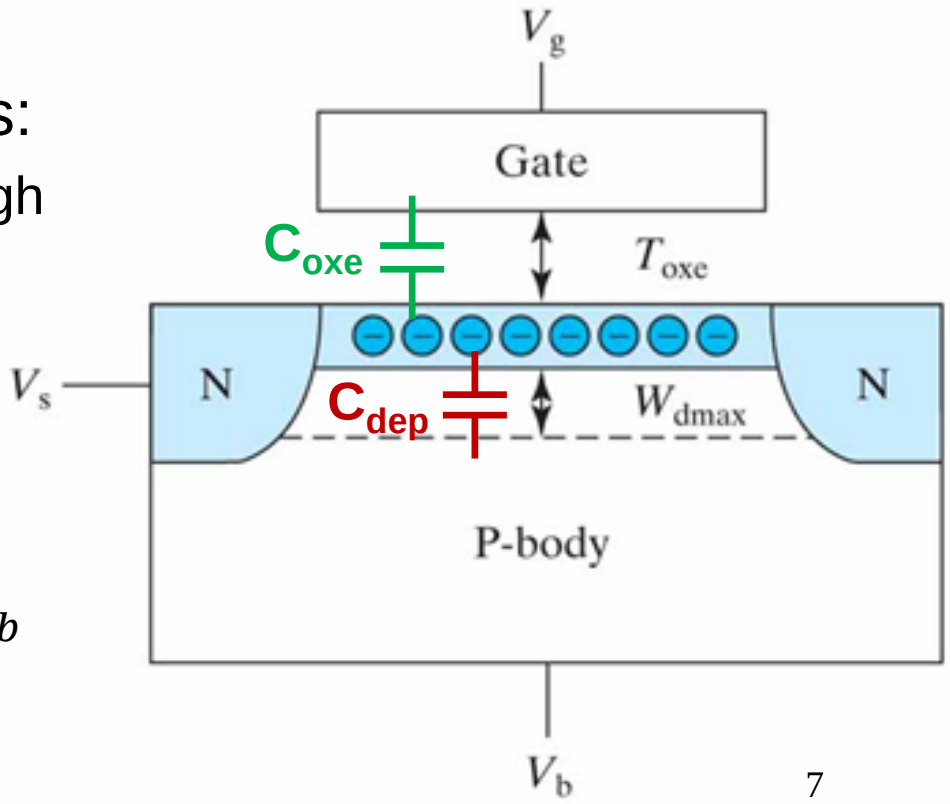
- What is the surface mobility at $V_{gs} = 1V$ in an N-channel MOSFET with $V_t = 0.3\ V$ and $T_{oxe} = 2\ nm$?

Body Effect

- Until now, we have assumed that the body and channel (inversion layer of MOS capacitor) are held at zero volts
- In MOS transistor, (channel potential) ≥ (source potential)
- What happens if source (or channel) is positive with respect to body (i.e. $V_{sb} > 0$)?
- There are now two capacitors:
  - one from gate to channel through the oxide
  - a second from channel to body through depletion layer silicon
- Now:

$$Q_{inv} = -C_{oxe}\left(V_{gs} - V_t\right) + C_{dep}.V_{sb}$$

where $C_{dep} = \dfrac{\varepsilon_s}{W_{dmax}}$



Body Effect on Threshold Voltage

$$Q_{inv} = -C_{oxe}\left(V_{gs} - V_t\right) + C_{dep}.V_{sb}$$

$$= -C_{oxe}\left(V_{gs} - \left(V_t + \frac{C_{dep}}{C_{oxe}}.V_{sb}\right)\right)$$

$$= -C_{oxe}\left(V_{gs} - V_t(V_{sb})\right)$$

$$V_t(V_{sb}) = V_{t0} + \frac{C_{dep}}{C_{oxe}}.V_{sb} = V_{t0} + \alpha.V_{sb}$$

$$\alpha = C_{dep}/C_{oxe} \approx (3T_{oxe})/W_{dmax}$$

- When source-body junction is reversed biased:
  - NFET V_t becomes more positive
  - PFET V_t becomes more negative
- This is known as body effect or back gate bias effect
  - α is the body effect coefficient

Uniform Body Doping

- Earlier generations MOS technology used uniform body doping
- Complicates expression for body effect because W_{dmax} is a function of V_{sb}
- V_t can be obtained by replacing $2\emptyset_B$ term (in expression for threshold voltage – previous lecture) with $(2\emptyset_B + V_{sb})$ which yields:

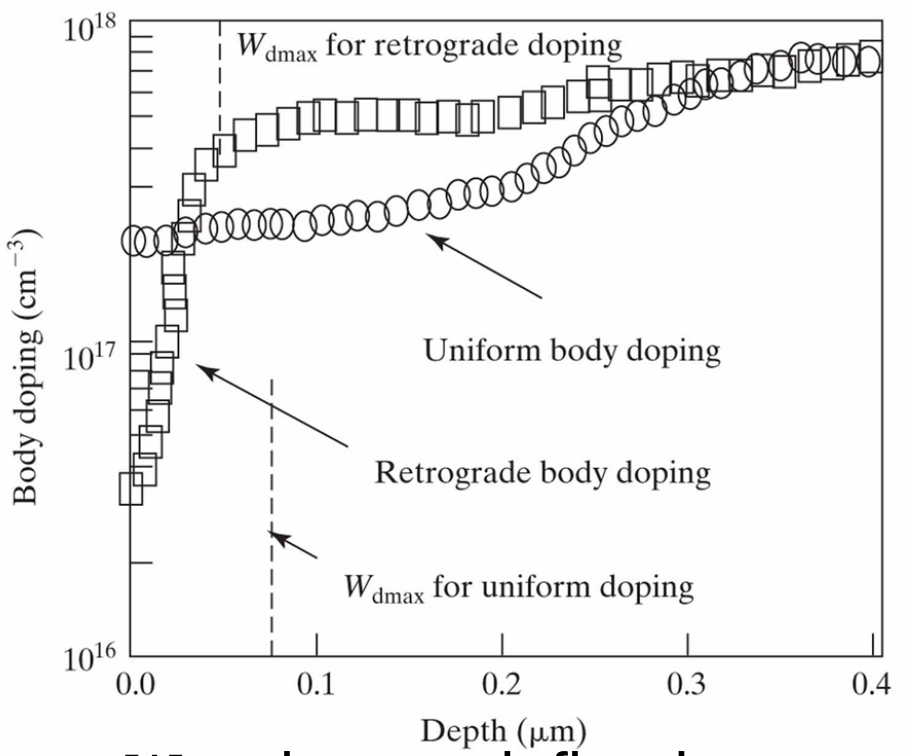
$$V_t = V_{t0} + \frac{\sqrt{2q.N_a.\varepsilon_s}}{C_{oxe}}\left(\sqrt{2\emptyset_B + V_{sb}} - \sqrt{2\emptyset_B}\right)$$

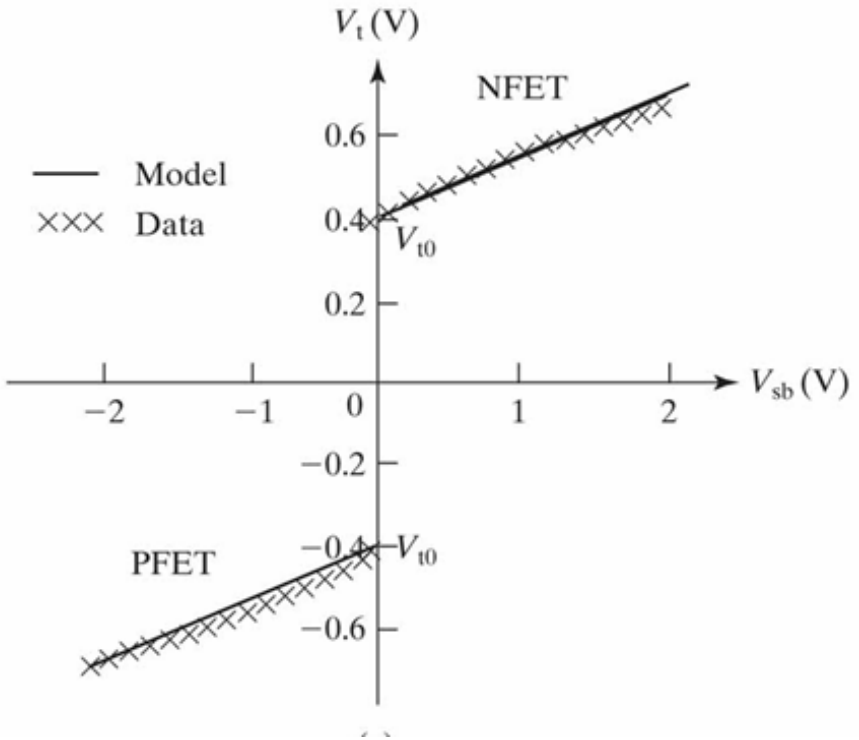
$$= V_{t0} + \gamma\left(\sqrt{2\emptyset_B + V_{sb}} - \sqrt{2\emptyset_B}\right)$$

- This is the "classical" formula for body-effect V_t variation
- γ is called body-effect parameter
  - sub-linear function of V_{sb}

Retrograde Body Doping

- Modern transistors employ steep retrograde body doping
  - light doping in surface layer with heavy doping underneath
- Reduces off-state leakage and improves surface mobility





- W_{dep} is now defined geometrically and independent of V_{sb}
- α is now constant ⇨ linear relation between V_t and V_{sb}

MOSFET IV – Very Small V_{ds}

- Consider MOS transistor with $V_{gs} > V_t, V_{ds} > 0$ but $V_{ds} \approx 0$
- Q_{inv} will be uniform along channel

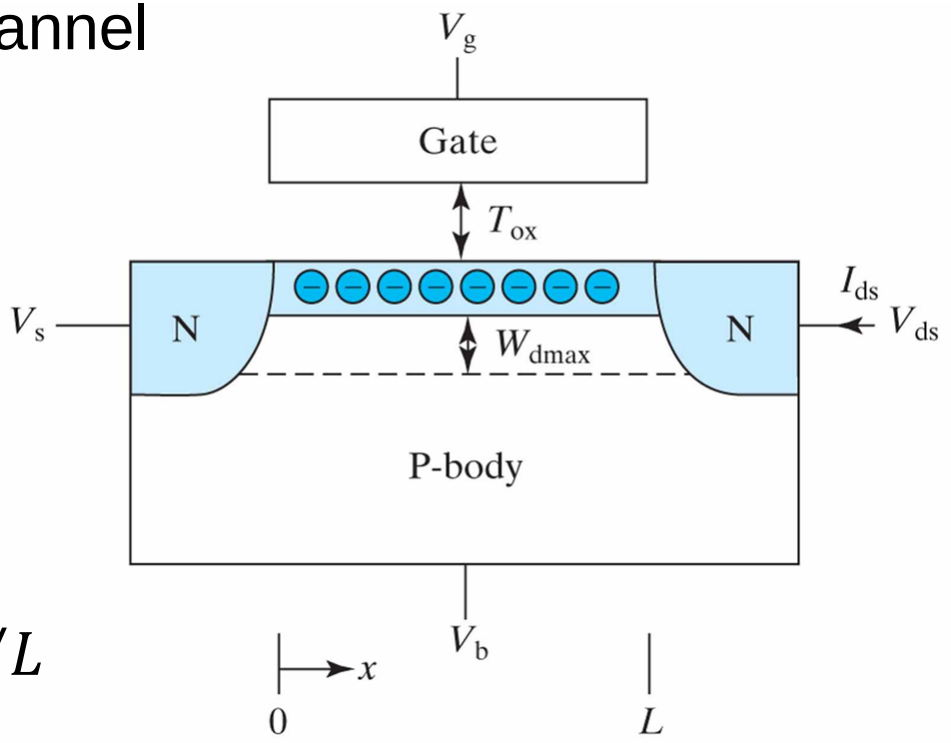
$$I_{ds} = W.Q_{inv}.v$$

where W is channel width

$$I_{ds} = W.Q_{inv}.\mu_{ns}.\overrightarrow{E_x}$$

$$= W.Q_{inv}.\mu_{ns}.V_{ds}/L$$

$$= W.C_{oxe}(V_{gs} - V_t).\mu_{ns}.V_{ds}/L$$



$$I_{ds} = \frac{W}{L}.C_{oxe}.\mu_{ns}.(V_{gs} - V_t).V_{ds}$$

MOSFET IV – Beta

- MOS transistors are sometimes characterized by a gain factor β

- For very small V_{ds}:

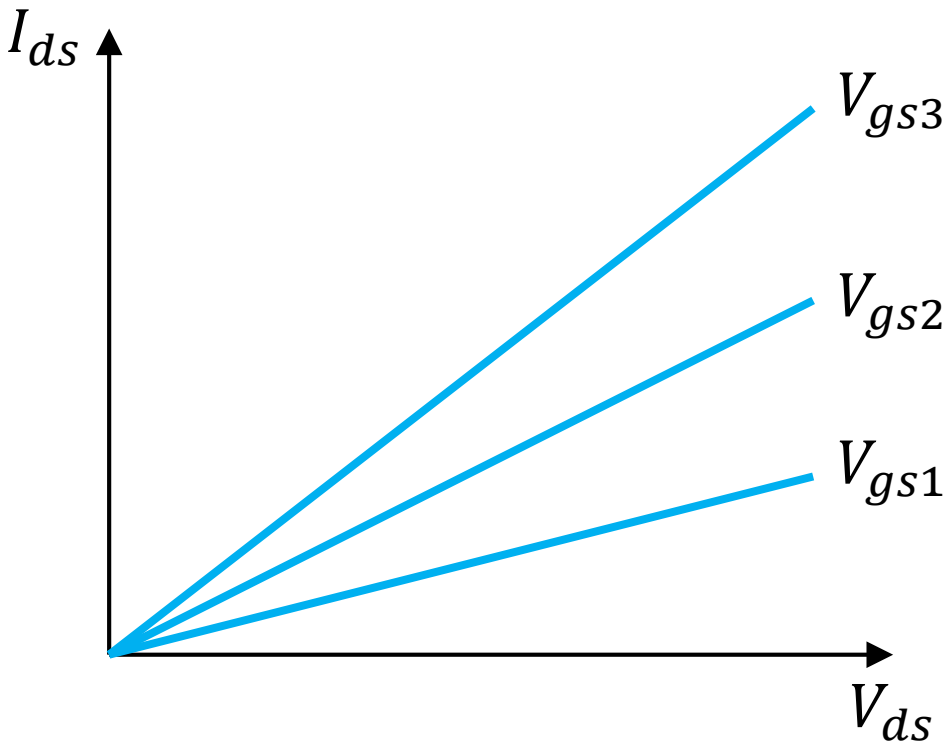
$$I_{ds} = \frac{W}{L}.C_{oxe}.\mu_{ns}.\left(V_{gs} - V_t\right).V_{ds} = \beta.\left(V_{gs} - V_t\right).V_{ds}$$

where $\beta = \frac{W}{L}.C_{oxe}.\mu_{ns}$

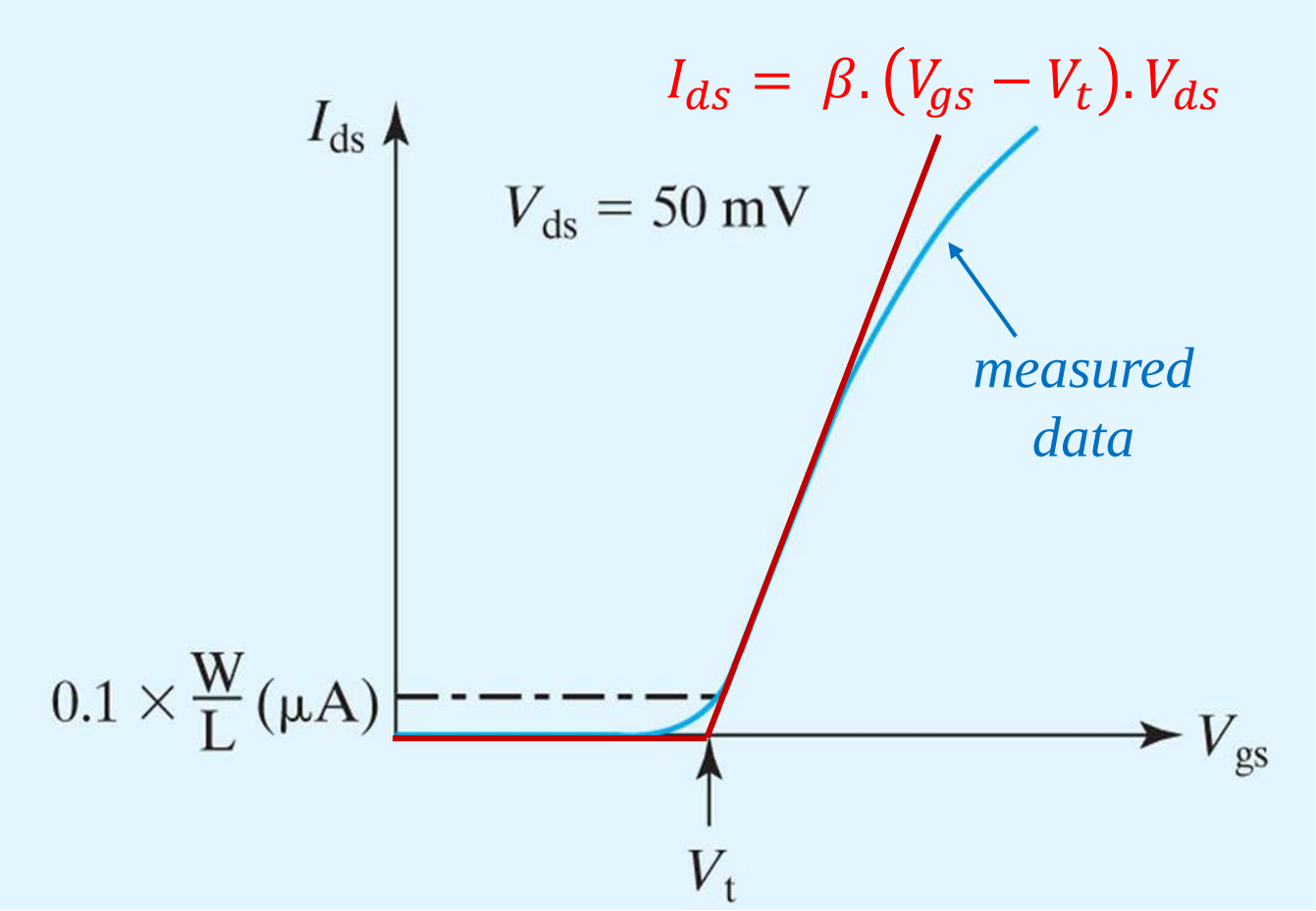
β captures physical and material properties of the transistor

MOSFET IV Characteristic – very small Vds

- For very small V_{ds}: $I_{ds} = \beta.(V_{gs} - V_t).V_{ds}$
  - If $V_{gs} < V_t$, $I_{ds} = 0$
  - If $V_{gs} > V_t$, MOSFET behaves as a linear resistor whose conductance is proportional to $(V_{gs} - V_t)$



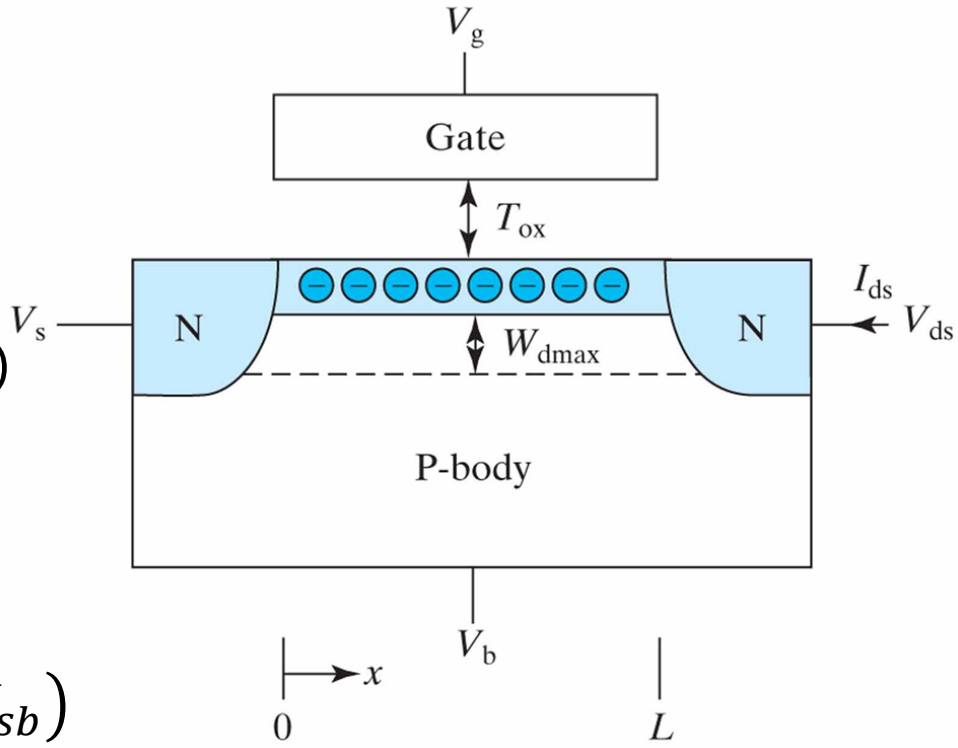
Measuring Threshold Voltage



- Empirical V_t can be determined by:
  a) extrapolating I_{ds} vs. V_{gs} curve to $I_{ds} = 0$
  b) measuring V_{gs} at which $I_{ds} = 0.1\mu A \times (W/L)$

Inversion Charge in MOSFET

- Now consider MOSFET with $V_{ds} > 0$ (and no longer very small)
- Channel voltage V_c is now a function of x
  - $V_c(0) = V_s$ or $V_{cs}(0) = 0$
  - $V_c(L) = V_d$ or $V_{cs}(L) = V_{ds}$
- As we move toward the drain
  - less voltage across oxide (& more across depletion layer)
  - fewer electrons (less charge density) in inversion layer



$$Q_{inv} = -C_{oxe}\left(V_g - V_{t0} - \alpha.V_{sb}\right)$$

becomes:

$$Q_{inv}(x) = -C_{oxe}\left(V_{gc}(x) - V_{t0} - \alpha.V_{cb}(x)\right)$$

Bulk Charge Factor

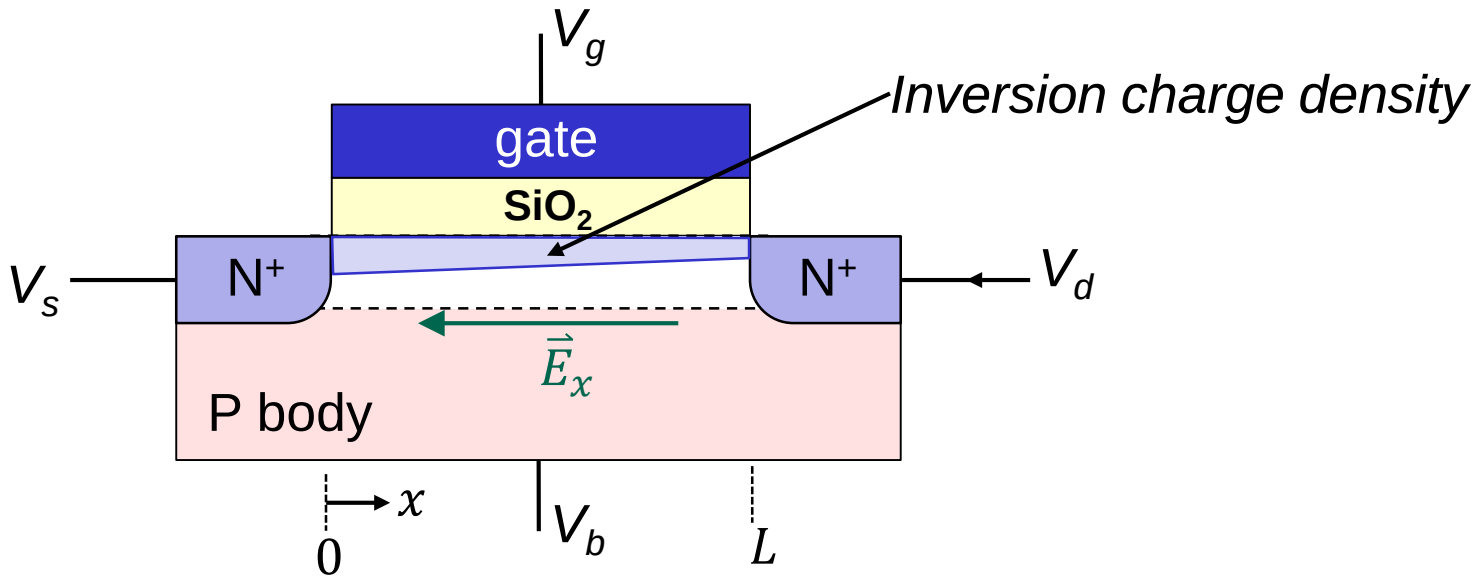
$$
\begin{aligned}
Q_{inv}(x) &= -C_{oxe}\left(V_{gc}(x) - V_{t0} - \alpha.V_{cb}(x)\right) \\
&= -C_{oxe}\left(V_{gs} - V_{cs}(x) - V_{t0} - \alpha(V_{cs}(x) + V_{sb})\right) \\
&= -C_{oxe}\left(V_{gs} - V_{cs}(x) - (V_{t0}+\alpha V_{sb}) - \alpha.V_{cs}(x)\right) \\
&= -C_{oxe}\left(V_{gs} - m.V_{cs}(x) - V_t\right)
\end{aligned}
$$

where $m \equiv (1+\alpha) = 1 + C_{dep}/C_{oxe} = 1 + 3(T_{oxe}/W_{dmax})$

- m is called body effect factor or bulk charge factor
- m is typically around 1.2
- First order models often use m=1

Channel Voltage Profile

- We know that $V_{cs}(0) = 0$ and $V_{cs}(L) = V_{ds}$
- What is $V_{cs}(x)$ for $0 < x < L$?
- Many simple analyses assume $V_{cs}(x) = x.V_{ds}/L$
  - inversion charge density decreases linearly from source to drain
  - horizontal electric field $\vec{E}_x = dV_{CS}/dx$ is constant



- This cannot be correct as $I_{ds} \propto Q_{inv}(x).\vec{E}_x(x)$ must be constant!
- $V_{cs}(x)$ is a much more complex function of x

MOSFET IV – Linear Region

- Fortunately, we can determine I_{ds} without knowing $V_{cs}(x)$
- We know $I_{ds} = W.Q_{inv}(x).v(x) = W.Q_{inv}(x).\mu_{ns}.\vec{E}_x(x)$

so $I_{ds}.dx = W.C_{oxe}\left(V_{gs} - m.V_{cs}(x) - V_t\right).\mu_{ns}.\vec{E}_x(x).dx$

$$= W.C_{oxe}\left(V_{gs} - m.V_{cs}(x) - V_t\right).\mu_{ns}.dV_{cs}$$

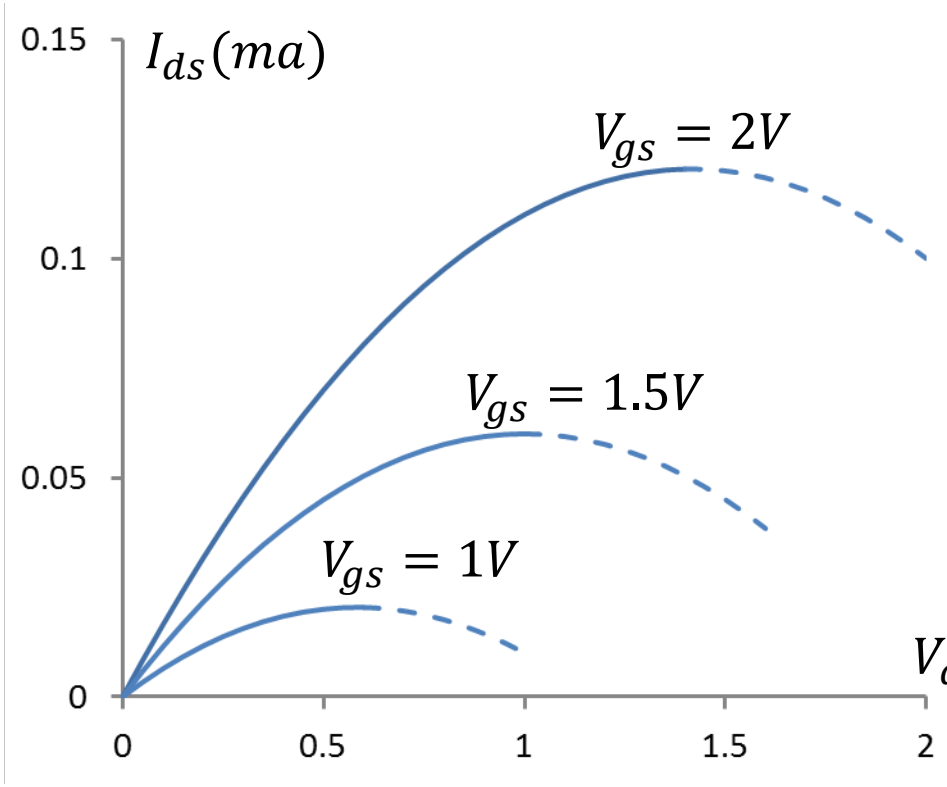
$$\int_0^L I_{ds}.dx = W.C_{oxe}.\mu_{ns}\int_0^{V_{ds}}\left(V_{gs} - m.V_{cs}(x) - V_t\right).dV_{cs}$$

$$I_{ds}.L = W.C_{oxe}.\mu_{ns}\left[\left(V_{gs} - V_t\right).V_{cs} - \frac{m.{V_{cs}}^2}{2}\right]_{V_{cs}=0}^{V_{cs}=V_{ds}}$$

$$I_{ds} = \frac{W}{L}.C_{oxe}.\mu_{ns}.\left(V_{gs} - V_t - \frac{m}{2}.V_{ds}\right).V_{ds}$$

$$= \beta.\left(V_{gs} - V_t - \frac{m}{2}.V_{ds}\right).V_{ds}$$

MOSFET IV – Linear Region



$$I_{ds} = \beta.\left(V_{gs} - V_t - \frac{m}{2}.V_{ds}\right).V_{ds}$$

- For small V_{ds}, I_{ds} increases linearly – behaves as a resistor
- As V_{ds} increases, charge in channel decreases
  - as a result: dI_{ds}/dV_{ds} decreases
- What happens when I_{ds} reaches it maximum ?

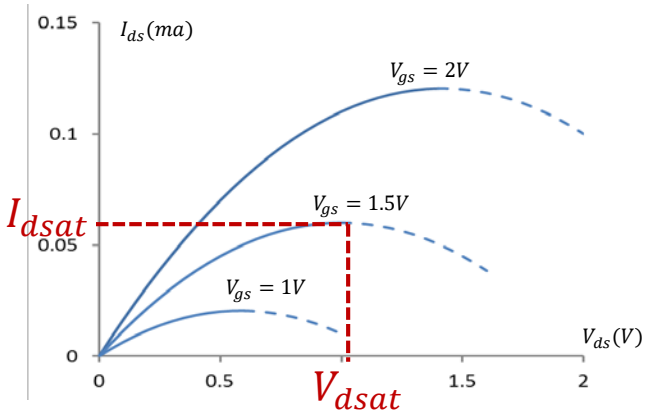
Drain Saturation Voltage

- At what point does I_{ds} reach it maximum?

$$I_{ds} = \beta.\left(V_{gs} - V_t - \frac{m}{2}.V_{ds}\right).V_{ds}$$

- Differentiating and setting to zero:

$$\frac{\partial I_{ds}}{\partial V_{ds}} = \beta.(V_{gs} - V_t - m.V_{ds}) = 0$$



- This gives:

$$V_{dsat} = \frac{V_{gs} - V_t}{m}$$

V_{dsat} is called the drain saturation voltage

- The drain current I_{ds} when $V_{ds} = V_{dsat}$ is given by:

$$I_{dsat} = I_{ds}(V_{dsat}) = \frac{W}{2m.L} C_{oxe}.\mu_{ns}.\left(V_{gs} - V_t\right)^2$$

or

$$I_{dsat} = \frac{\beta}{2m}\left(V_{gs} - V_t\right)^2$$

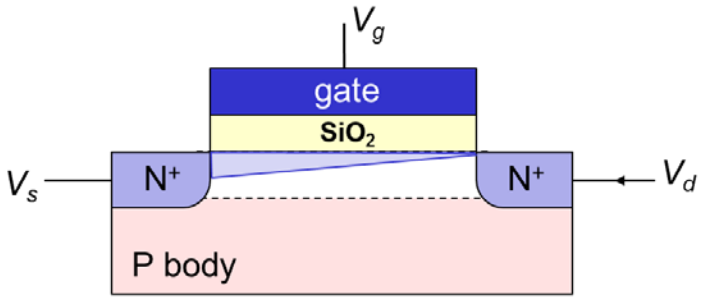
I_{dsat} is called the drain saturation current

- Note that V_{dsat} and I_{dsat} are both functions of V_{gs}

Saturation

- What causes the current to “max-out” at V_{dsat}?
- Charge in channel is: $Q_{inv}(x) = -C_{oxe}\left(V_{gs} - m.V_{cs}(x) - V_t\right)$
- At saturation, $V_{cs}(x)$ at the drain end of channel is $V_{cs}(L) = V_{dsat}$
- Substituting into the equation above:

$$Q_{inv}(L) = 0 \text{ when } V_{ds} = V_{dsat}$$

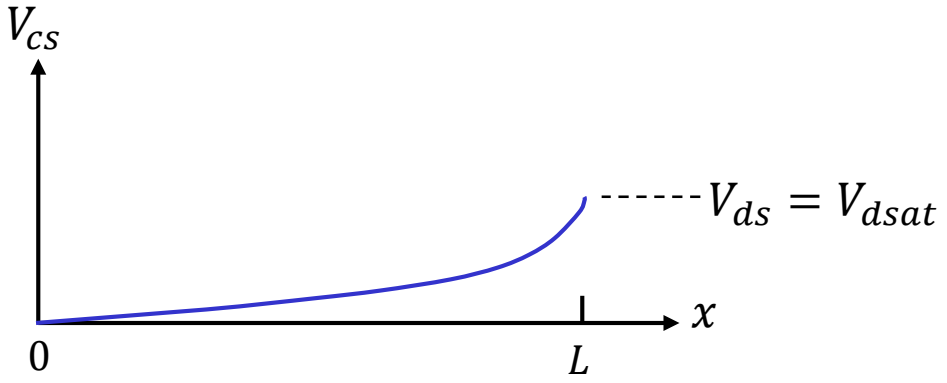


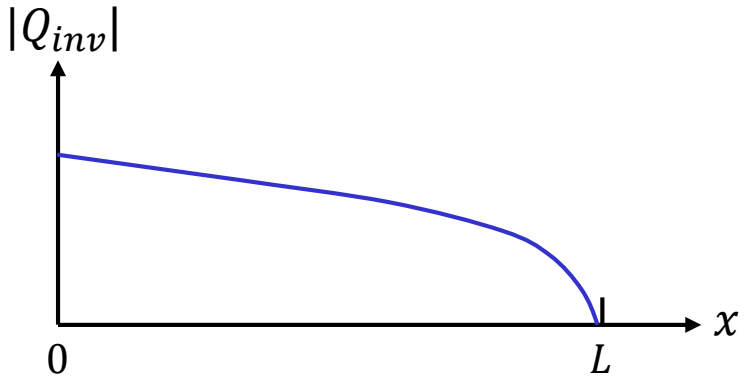
- i.e., the inversion charge density at the drain end of the channel has been reduced to zero!
- Disappearance of the inversion layer is called channel pinch-off

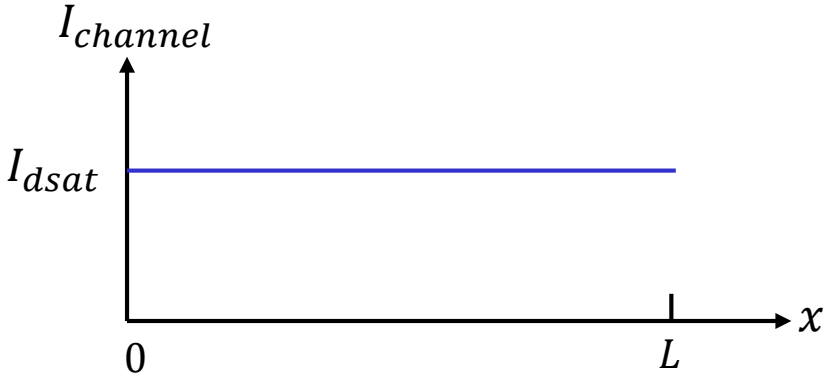
Voltage & Charge in Channel at Saturation

$$|Q_{inv}| = C_{ox}\left(V_g - m.V_{cs} - V_t\right)$$

$$I_{channel} = \mu_{ns}.Q_{inv}.\frac{dV_{cs}}{dx}$$

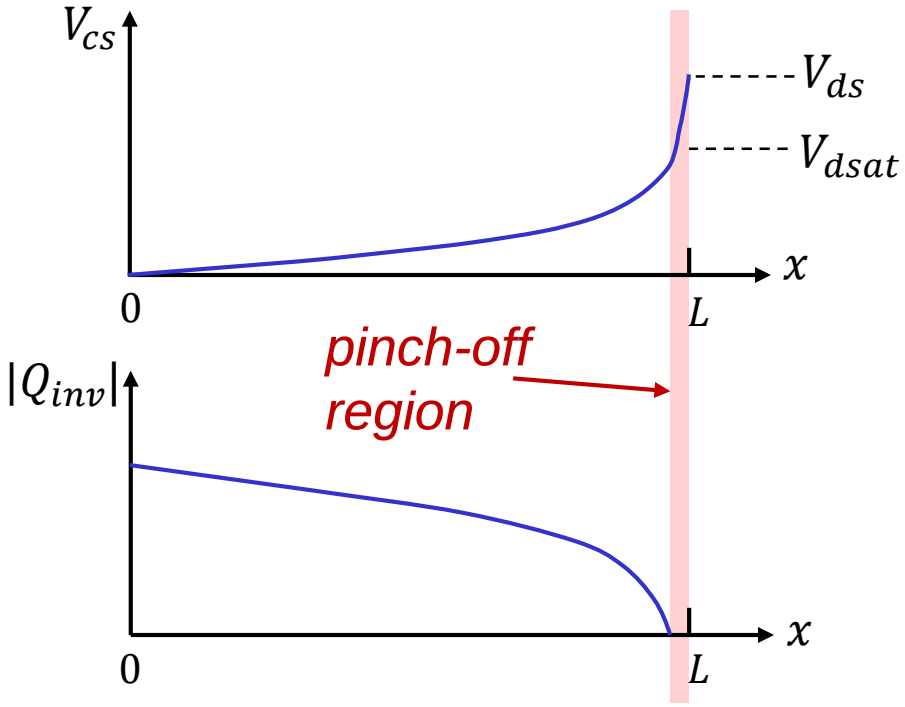






Saturation Region

- What happens when V_{ds} is increased beyond V_{dsat}?
- Pinch-off region (i.e. the region where the channel charge density is zero) now extends a short finite distance from the drain toward the source
- Pinch-off region is a high-field region across which the voltage $V_{ds} - V_{dsat}$ is dropped



Note that because the pinch-off region is very small, $V_{cs}(x)$ and $Q_{inv}(x)$ are almost identical to what they were when $V_{ds} = V_{dsat}$

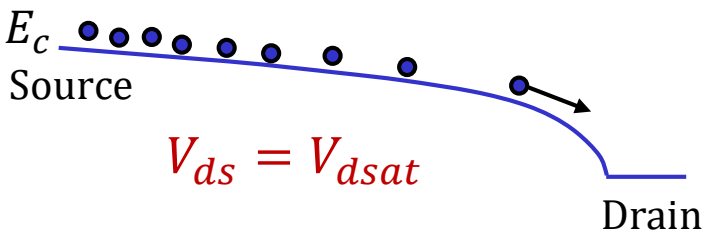
But $I_{channel} = \mu_{ns}.Q_{inv}.\dfrac{dV_{cs}}{dx}$

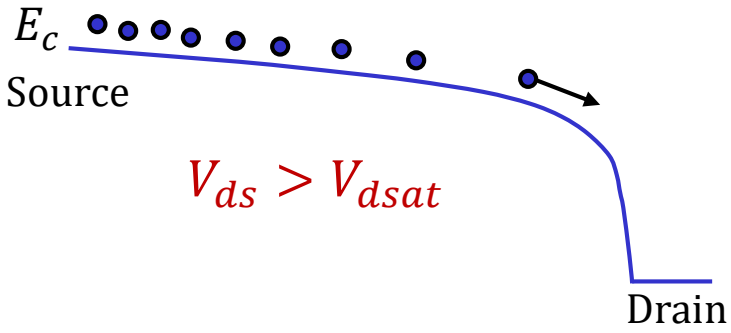
As a result:

$$I_{ds} = I_{dsat} \quad \text{for} \quad V_{ds} \geq V_{dsat}$$

Saturation Region

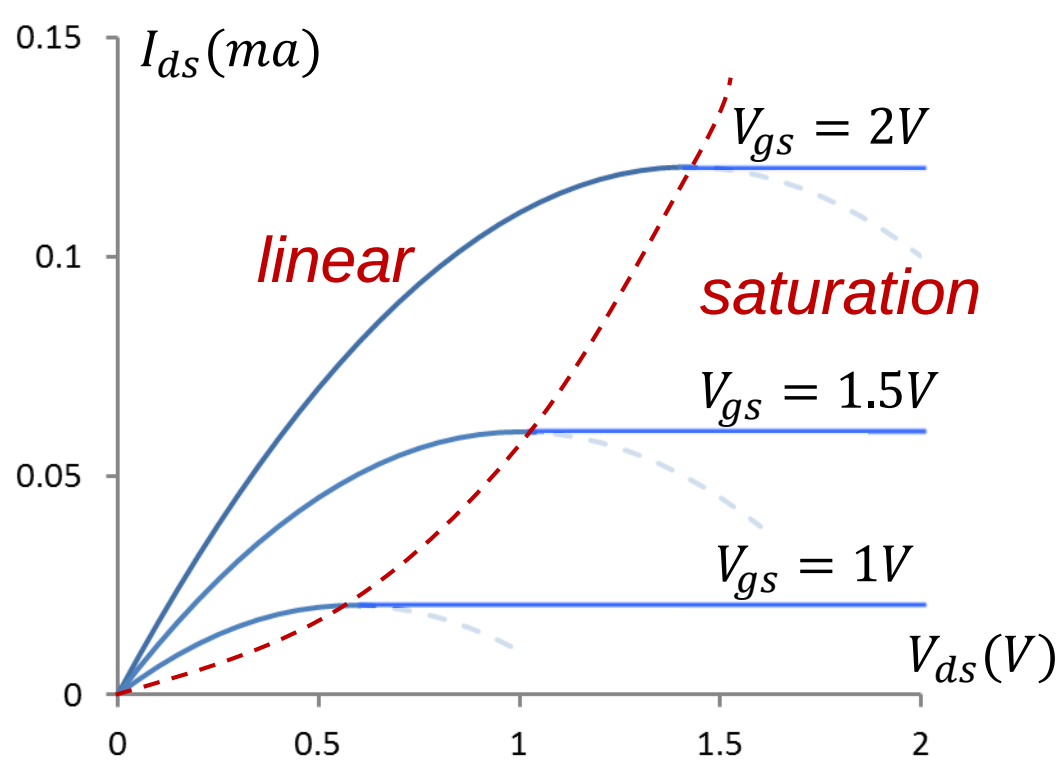
- MOSFET acts as a constant current source in saturation
- How can current flow through pinch-off region if there is no inversion charge?
- Pinch-off region is a depletion region
- Depletion region is not a barrier to current flow
  - Current can flow across depletion region if there is an electric field and there is a source of carriers (as in PN diode)
  - When electrons reach pinch-off region, they are swept across this region by the strong electric field





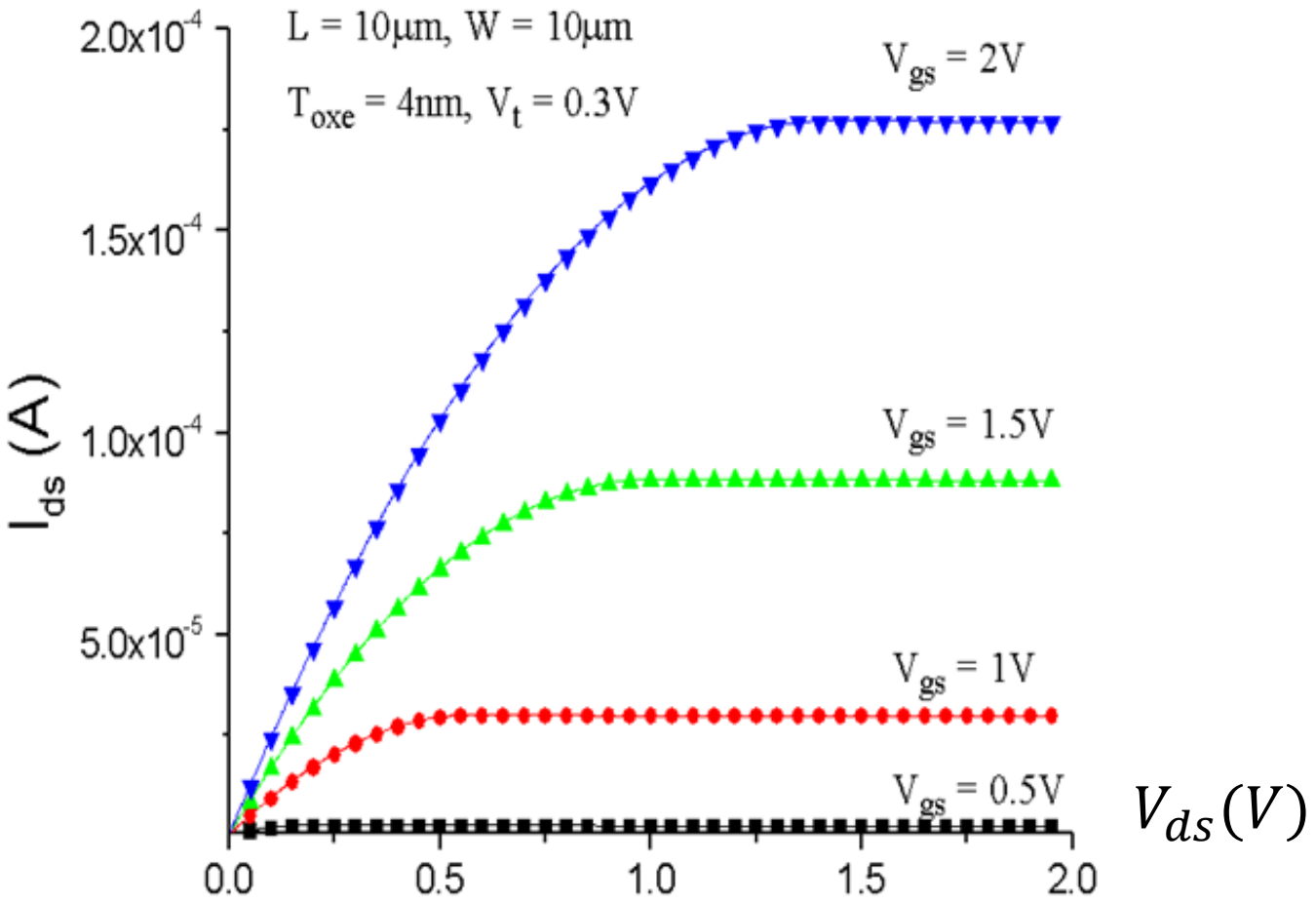
- Waterfall analogy
  - flow down waterfall is independent of height of waterfall

MOSFET IV – Linear & Saturation Regions



- For small V_{ds}, I_{ds} increases linearly – behaves as a resistor
- As V_{ds} increases, charge in channel decreases
  - as a result: dI_{ds}/dV_{ds} decreases
- When V_{ds} reaches $V_{dsat} = (V_{gs} - V_t)/m$, pinch-off occurs
  - $I_{ds} = I_{dsat}$ - transistor behaves as constant current source

MOSFET IV – Long Channel Model



- Equations we have developed sometimes known as first-order model or Shockley model (esp. with m=1), or long-channel model
- Accurately describe behavior of long-channel MOSFETs

Transconductance

- In saturation region, MOSFET behaves as a voltage controlled constant current source
- Convenient to describe “gain” of the transistor in terms of its transconductance:

$$g_m = \frac{\partial I_{ds}}{\partial V_{gs}} = \frac{W}{m.L}.C_{oxe}.\mu_{ns}\left(V_{gs} - V_t\right)$$

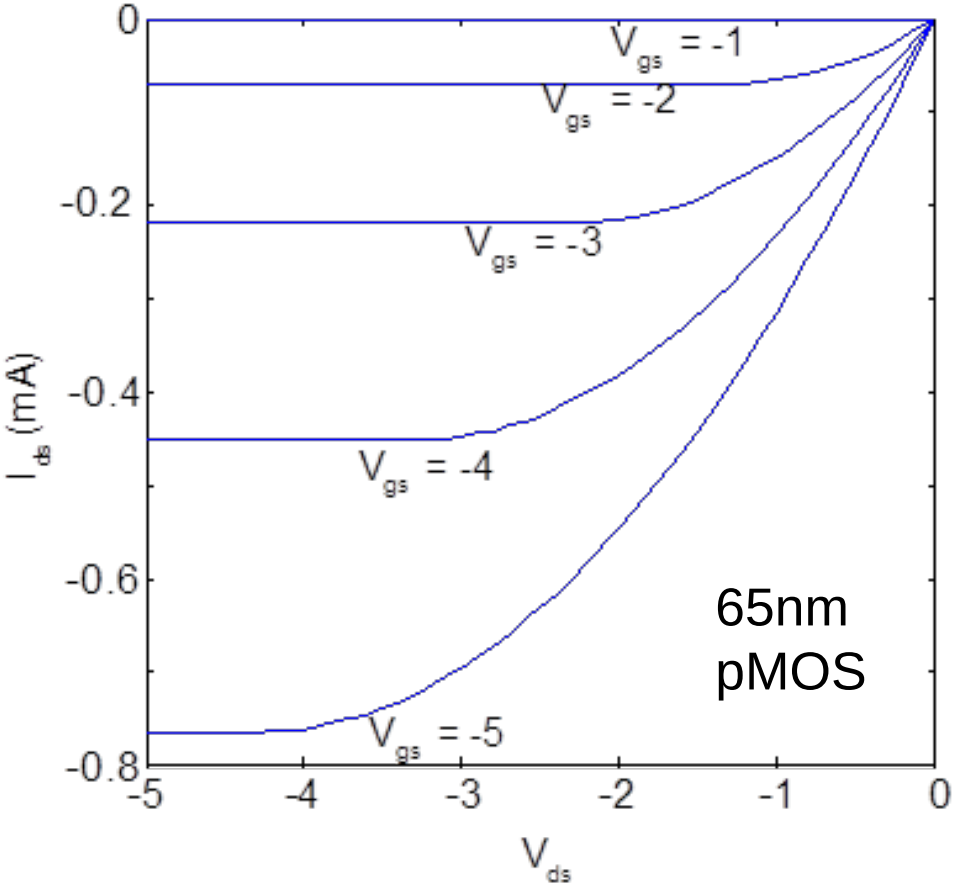
$$\boxed{g_m = \frac{\beta}{m}\left(V_{gs} - V_t\right)}$$

Summary of NMOS Long Channel Model

Cut-Off	$V_{gs} < V_t$	$I_{ds} = 0$
Linear	$V_{gs} > V_t$ $V_{ds} < V_{dsat}$	$I_{ds} = \beta . \left(V_{gs} - V_t - \frac{m}{2} . V_{ds} \right) . V_{ds}$
Saturation	$V_{gs} > V_t$ $V_{ds} > V_{dsat}$	$I_{ds} = \frac{\beta}{2m} (V_{gs} - V_t)^2$ $g_m = \frac{\beta}{m} (V_{gs} - V_t)$

PMOS Long Channel Model

- All dopings and voltages are inverted for PMOS
  - Source is the more positive terminal
  - $V_{gs},\ V_{ds},\ V_{dsat},\ V_t$ and I_{ds} are all ≤ 0



- Mobility determined by holes
  - μ_{ps} typically 2-3x lower than that of electrons μ_{ns}

$$\beta = \frac{W}{L}.C_{oxe}.\mu_{ps}$$

- PMOS transistors must be 2-3 times wider to provide the same drive current

Summary of PMOS Long Channel Model

- Note that in PMOS transistor:

  $V_{gs},\ V_{ds},\ V_{dsat},\ V_t$ and I_{ds} are all ≤ 0

Cut-Off	$V_{gs} > V_t$	$I_{ds} = 0$
Linear	$V_{gs} < V_t$ $V_{ds} > V_{dsat}$	$I_{ds} = -\beta.\left(V_{gs} - V_t - \frac{m}{2}.V_{ds}\right).V_{ds}$
Saturation	$V_{gs} < V_t$ $V_{ds} < V_{dsat}$	$I_{ds} = \frac{-\beta}{2m}\left(V_{gs} - V_t\right)^2$ $g_m = \frac{-\beta}{m}\left(V_{gs} - V_t\right)$

Example:

- An ideal NMOS transistor has the following parameters:
  - $W = 50\mu m,\ L = 5\mu m$
  - $T_{oxe} = 25\ nm$
  - $W_{dmax} = 375nm$
  - $V_t = 0.4\ V$
  - $\mu_{ns} = 350\ cm^2/V.s$
- Determine:
  a) V_{dsat} , I_{dsat} and g_{msat} at $V_{gs} = 1, 2\ and\ 3V$
  b) Sketch I_{ds} *vs.* V_{ds} curves for $0 < V_{ds} < 3V$ and $V_{gs} = 1, 2\ and\ 3V$

Non-Ideal I-V Effects

- We will now examine non-ideal effects that detract from the behavior described by long-channel model:

- Velocity Saturation
- Channel Length Modulation
- Body Effect (we already covered this)
  - variation of threshold voltage with source-body bias

$$V_t = V_{t0} + \alpha . V_{sb} \quad where \quad \alpha = (m-1) \approx 3 . C_{oxe} / W_{dmax}$$

- Sub-threshold Current
- Drain Induced Barrier Lowering (DIBL)

Velocity Saturation

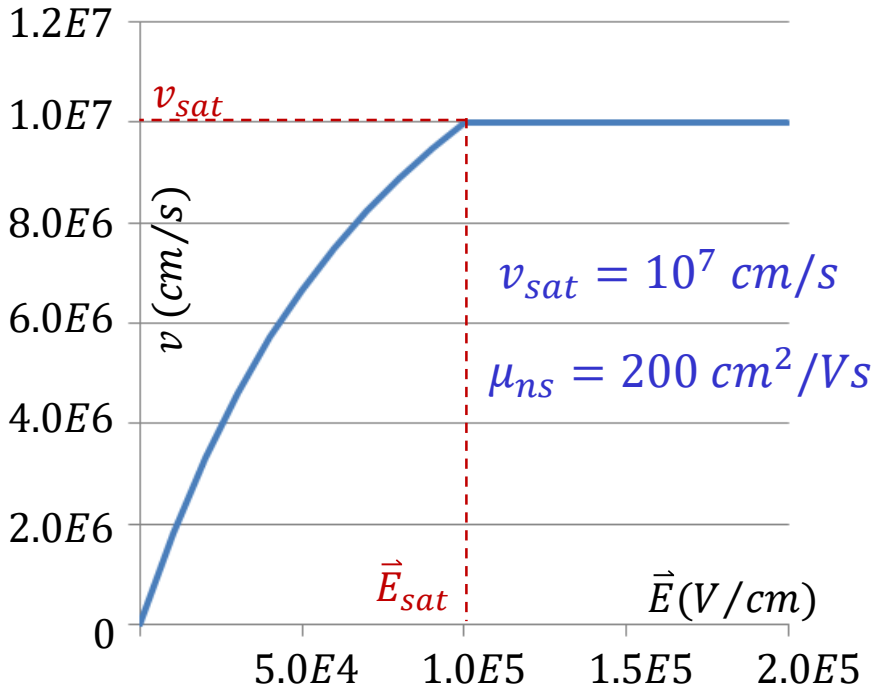
- In short channel length devices, electric field can be very high – leads to velocity saturation
  - particularly when device is in saturation and very high field exists in pinch-off region

- Empirically model velocity saturation as:

$$v = \frac{\mu_{ns}.\vec{E}}{1 + \vec{E}/\vec{E}_{sat}} \quad \text{for } \vec{E} \leq \vec{E}_{sat}$$

$$v = v_{sat} \quad \text{for } \vec{E} \geq \vec{E}_{sat}$$

- where $\vec{E}_{sat} \equiv 2.v_{sat}/\mu_{ns}$



MOS IV Model with Velocity Saturation

- Re-evaluating expressions for I_{ds} (linear) with saturation limited mobility gives:

$$I_{ds} = \frac{\beta\left(V_{gs} - V_t - \frac{m}{2}.V_{ds}\right).V_{ds}}{1 + V_{ds}/\left(\vec{E}_{sat}.L\right)} \qquad \text{for} \quad V_{ds} < V_{dsat}, \;\; v < v_{sat}$$

$$= \frac{\text{long-channel } I_{ds}}{1 + V_{ds}/\left(\vec{E}_{sat}.L\right)}$$

usually valid in linear range

- At onset of pinch-off and velocity saturation:

$$I_{ds} = I_{ds}(L) = W.Q_{inv}(L).v(L)$$

$$= W.C_{oxe}.\left(V_{gs} - V_t - m.V_{dsat}\right).v_{sat}$$

Saturation Voltage with Velocity Saturation

- Equating these two expressions for I_{ds} at $V_{ds} = V_{dsat}$ gives:

$$\frac{1}{V_{dsat}} = \frac{m}{V_{gs} - V_t} + \frac{1}{\vec{E}_{sat}.L}$$

- V_{dsat} is reduced by velocity saturation

- V_{dsat} is less than smaller of:
  - long-channel V_{dsat} and
  - that V_{ds} that would give an average electric field of $\vec{E}_{sat}$ along the length of the channel
  - (same math as two resistors in parallel)

Saturation Current with Velocity Saturation

- Substituting eqn. for V_{dsat} into (linear) expression for I_{ds}:

$$I_{dsat} = \frac{W}{2m.L}.C_{oxe}.\mu_{ns}.\frac{\left(V_{gs}-V_t\right)^2}{1+\frac{V_{gs}-V_t}{m.\vec{E}_{sat}.L}}$$

$$= \frac{\text{long-channel } I_{dsat}}{1+\frac{V_{gs}-V_t}{m.\vec{E}_{sat}.L}} \quad = \frac{\beta}{2}\left(V_{gs}-V_t\right).V_{dsat}$$

- Note that for long channel case or low V_{gs},

$$\vec{E}_{sat}.L \gg \left(V_{gs}-V_t\right)$$

  - this reverts simply to long channel model

Short Channel MOSFETs

- For the very short channel case: $\vec{E}_{sat}.L \ll (V_{gs} - V_t)$

$$V_{dsat} \approx \vec{E}_{sat}.L$$

$$I_{dsat} \approx W.v_{sat}.C_{oxe}(V_{gs} - V_t - m.\vec{E}_{sat}.L)$$

- Note that I_{dsat} is no longer proportional to $1/L$
- And $I_{dsat} \propto (V_{gs} - V_t)$ rather than $(V_{gs} - V_t)^2$
- In short-channel devices, pinch-off region becomes a velocity saturation region
- Velocity saturation is a serious limitation on the I_{on} of short channel MOSFETs

Example: Velocity Saturation

At V_{gs} = 1.8 V, what is the V_{dsat} and I_{dsat} of an NFET with W = 1μm, T_{oxe} = 3 nm, μ_{ns}=200 cm^2/Vs, v_{sat} = 8 x 10^6 cm/s, V_t = 0.25 V, and W_{dmax} = 45 nm for:

(a) L =10 μm

(b) L = 1 um

(c) L = 0.1 μm

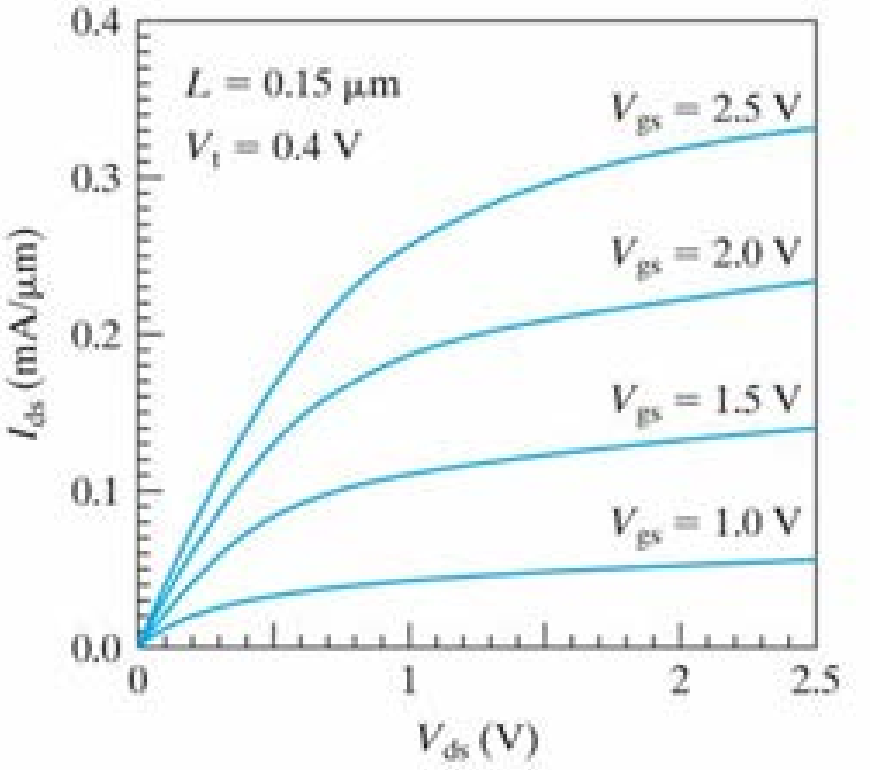
(d) L = 0.05 μm?

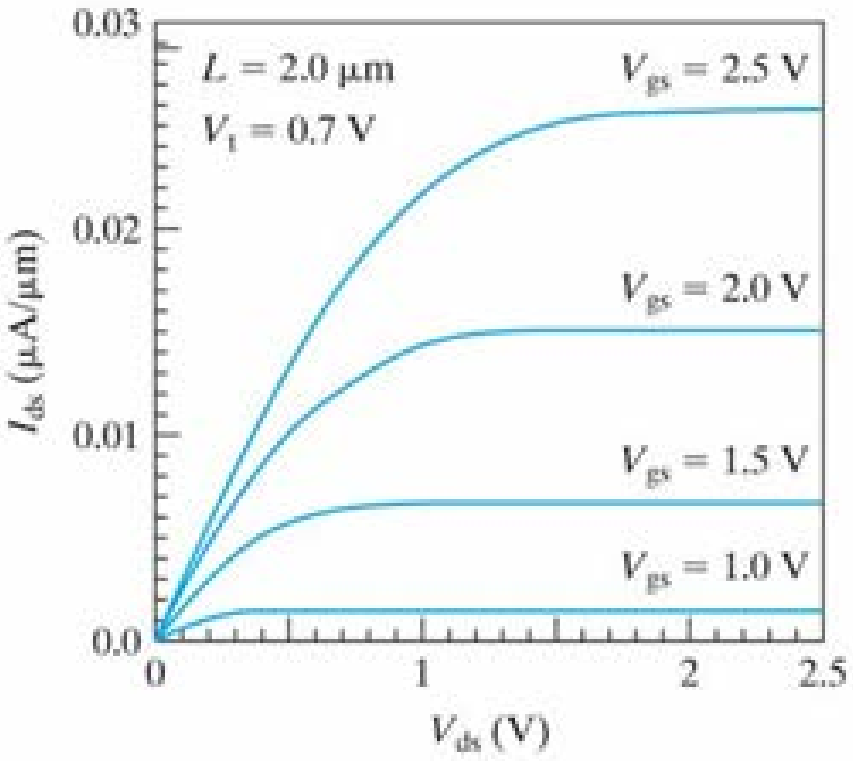
Compare to Long-Channel Model

Using data from previous example:

L (μm)	Long-channel		with Velocity Saturation	
	V_{dsat} (V)	I_{dsat} (μA)	V_{dsat} (V)	I_{dsat} (μA)
10	1.29	23.1	1.27	22.8
1	1.29	231	1.11	200
0.1	1.29	2310	0.494	882
0.05	1.29	4620	0.305	1090

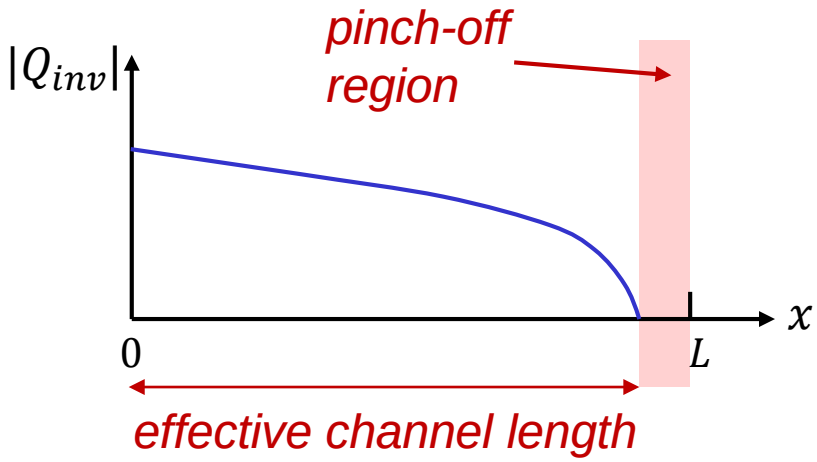
Compare Long & Short Channel MOSFETs





Channel Length Modulation

- Until now, we have assumed that length of pinch-off region does not significantly reduce length of channel
- In short channel length devices, as V_{ds} increases beyond V_{sat}, effective channel length decreases leading to an increase in I_{ds}



- I_{ds} increases with increasing V_{ds} - even in saturation
- Can be modeled as:

$$I_{ds} = \frac{\beta}{2m}\left(V_{gs} - V_t\right)^2.(1 + \lambda.V_{ds}) = I_{dsat}(1 + \lambda.V_{ds})$$

- where λ is channel length modulation parameter
  - units are V^{-1}

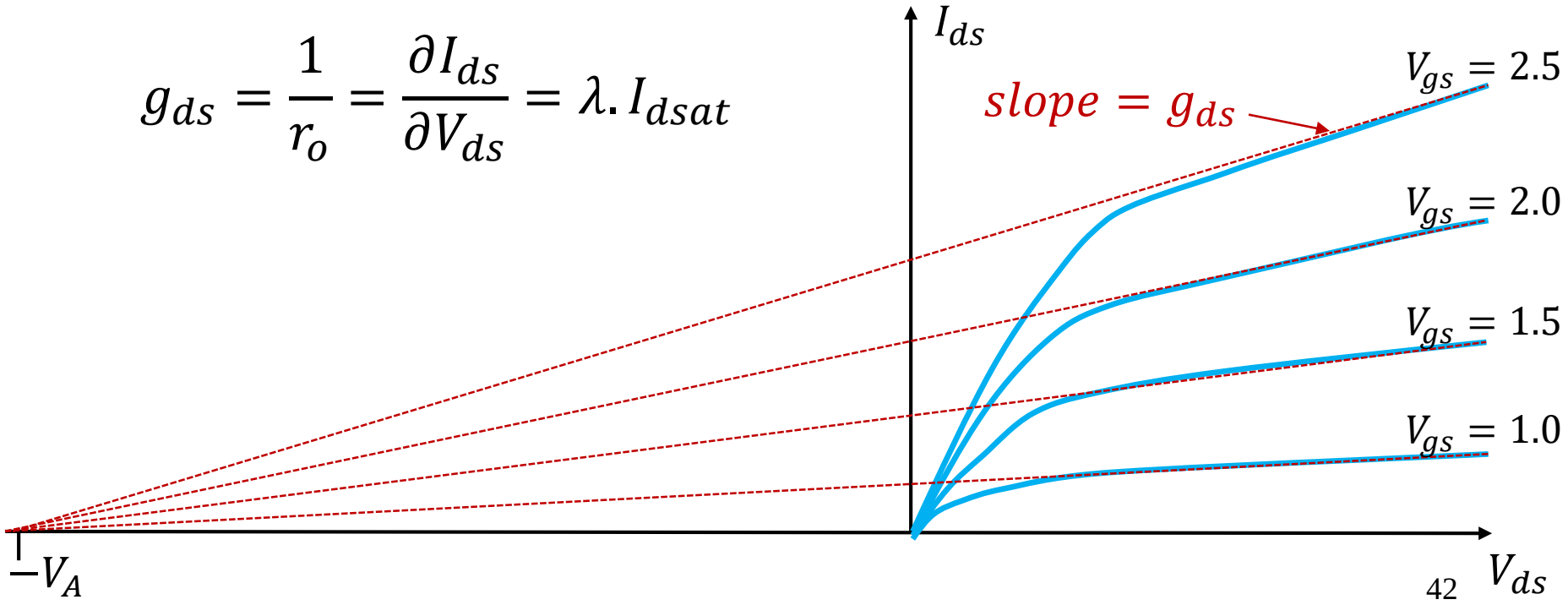
Output Conductance

- Like bipolar transistor, channel length modulation can also be modeled as an Early effect:

  $I_{ds} = V_{dsat}(1 + V_{ds}/V_A)$ where Early voltage $V_A = 1/\lambda$

- In saturation, small signal output conductance:

$$g_{ds} = \frac{1}{r_o} = \frac{\partial I_{ds}}{\partial V_{ds}} = \lambda . I_{dsat}$$



Example: MOS Amplifier

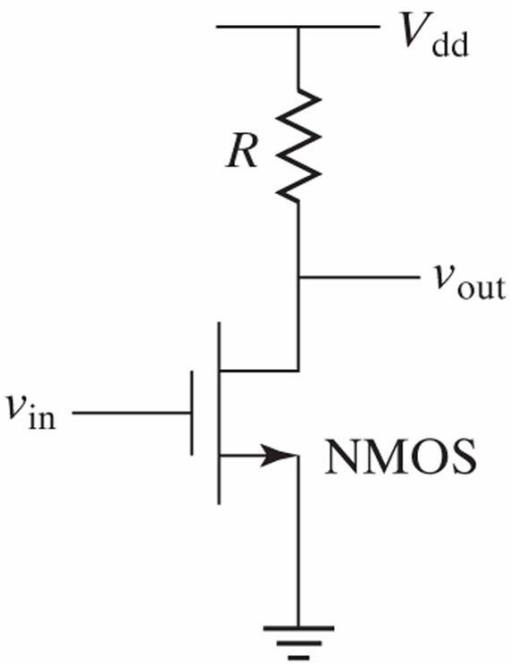
- An MOS transistor operates in the saturation region. A small signal input, v_{in} is applied.

$$i_{ds} = g_m . v_{gs} + g_{ds} . v_{ds}$$

$$= g_m . v_{in} + g_{ds} . v_{\text{out}}$$

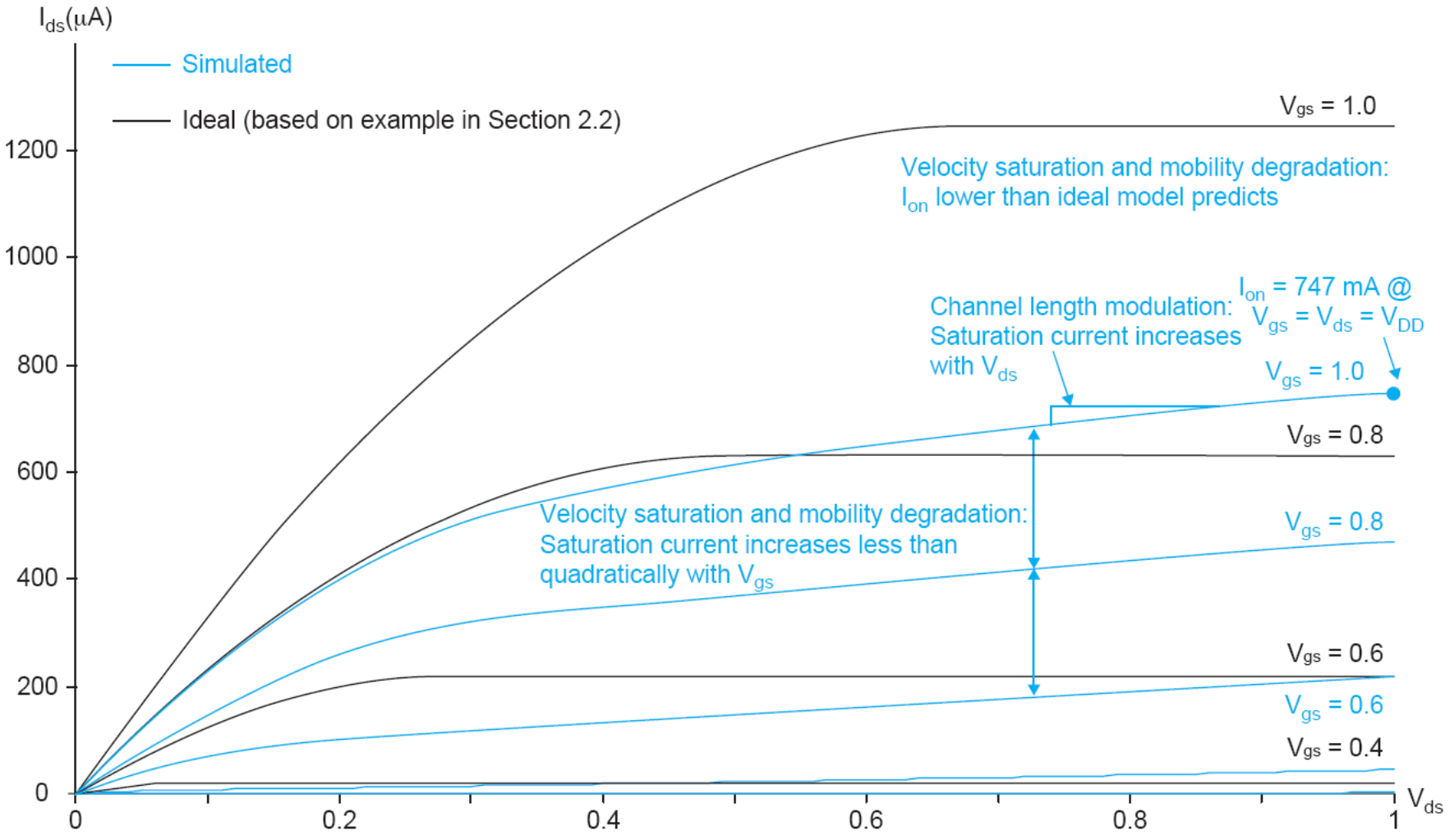
$$i_{ds} = -v_{out}/R$$

$$voltage\ gain = \frac{v_{out}}{v_{in}} = \frac{-g_m}{g_{ds} + 1/R}$$



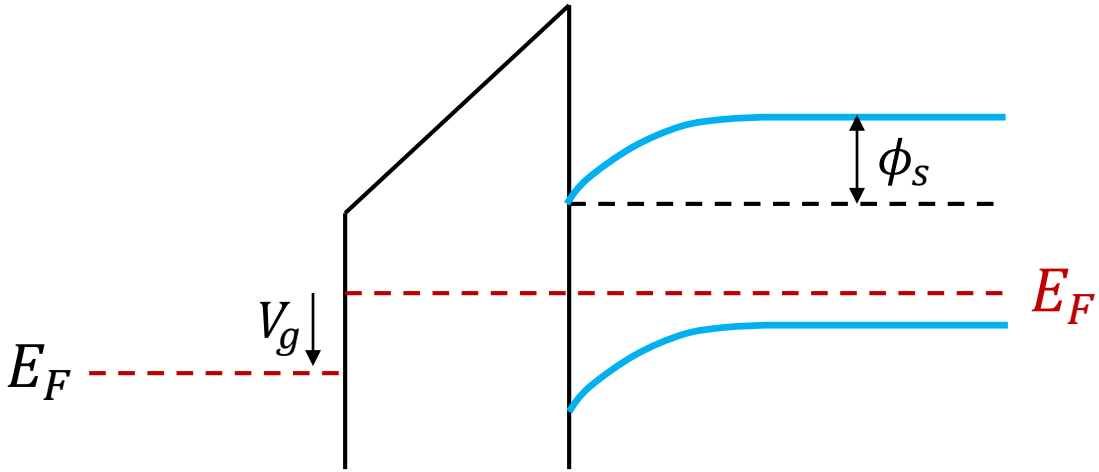
- A smaller g_{ds} is desirable for large voltage gain.
- Maximum available gain (or intrinsic voltage gain) is g_m/g_{ds}

Combined Short Channel Effects



Sub-threshold Conduction

- Until now, we have assumed $I_{ds} = 0 \;\; for \; V_{gs} < V_t$
- But a small positive V_{gs} will increase band bending and lower surface potential at silicon-oxide interface



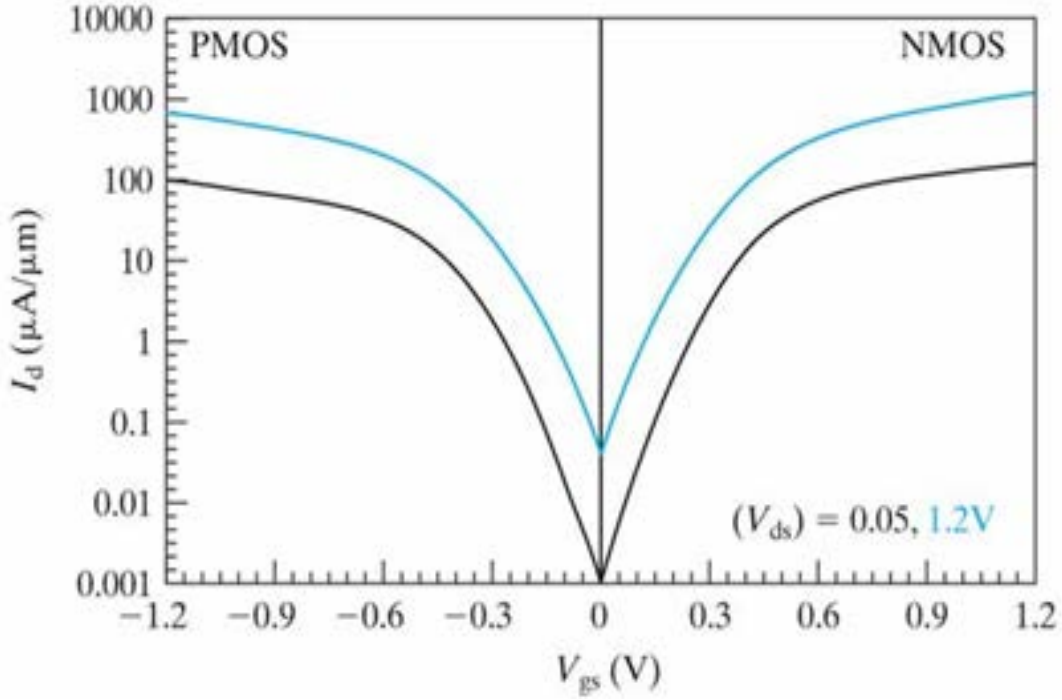
$\phi_s \approx constant + V_g/\eta$ where $\eta = 1 + C_{dep}/C_{oxe}$

$I_{ds} \propto n_s \propto e^{q.\phi_s/kT}$

$I_{ds} \propto e^{q.V_g/\eta kT}$ in sub-threshold

Sub-threshold Current

- In sub-threshold, current increases exponentially with V_{gs}
- Current relatively independent of V_{ds} for $V_{ds} >$ a few kT
- In short channel length devices, more sensitivity to V_{ds} as V_t is reduced at high V_{ds} through a process known as drain-induced barrier lowering of DIBL



Sub-threshold Current

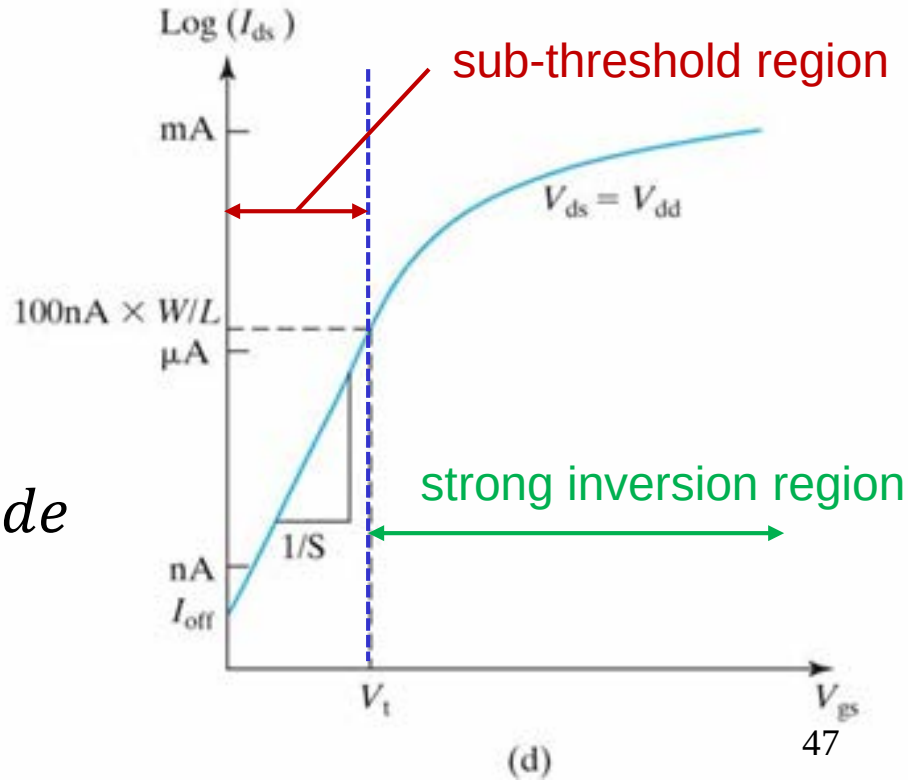
- Practical and common definition of V_t is the value of V_{gs} at which $I_{ds} = 100nA \times (W/L)$, then:

$$I_{ds}(nA) \approx 100.\frac{W}{L}.e^{q(V_{gs}-V_t)/\eta kT} \quad \text{for } V_{gs} < V_t \text{ and } V_{ds} \gg kT$$

- Plotting $ln(I_{ds})\, vs.\, V_{gs}$:
  - Sub-threshold slope

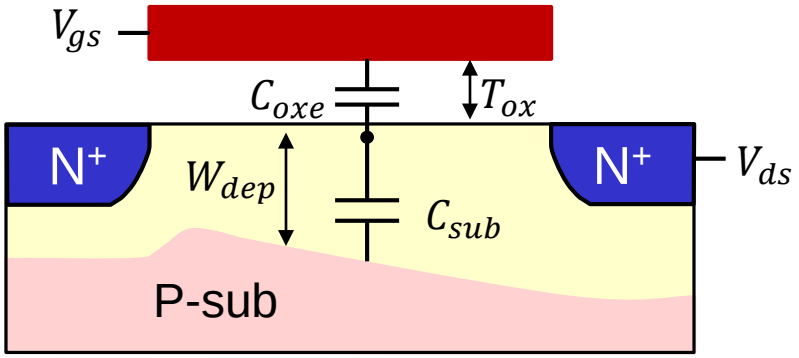
$$1/S = \eta kT/q$$

- S is typically $100\ mV/decade$ at room temperature



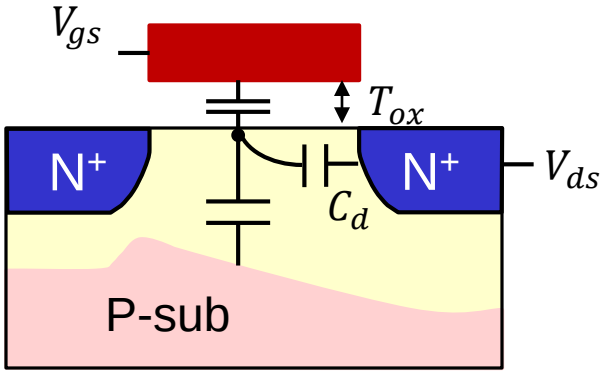
Drain Induced Barrier Lowering (DIBL)

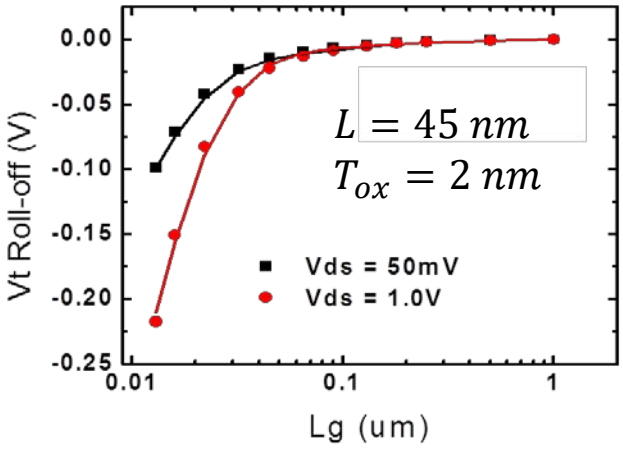
- In a long channel device, surface potential is influenced by both gate potential and body potential



this is the back-gate bias effect – increases V_T

- In a short channel device, surface potential is also influenced by close proximity of drain

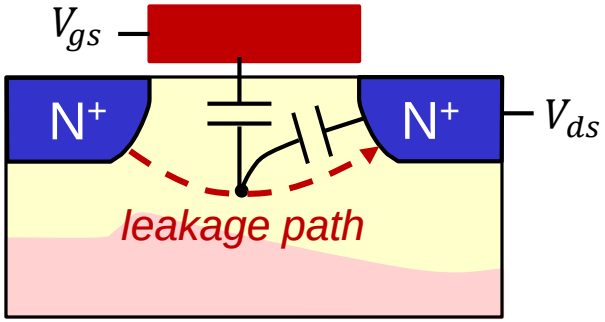




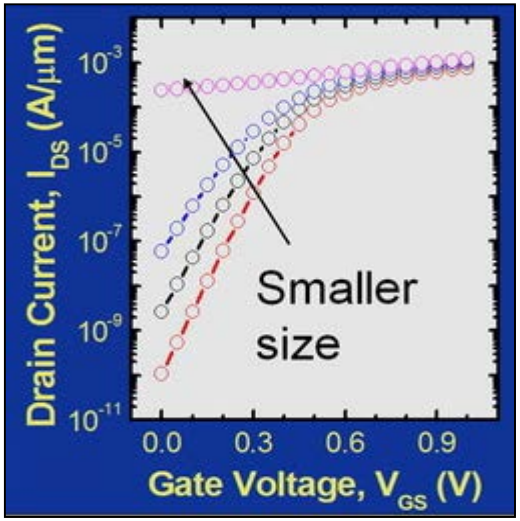
V_T is now a function of V_{ds}. Becomes harder to turn device off at high V_{ds}.

Sub-surface Leakage Paths

- Can reduce effect of drain on surface channel by increasing relative effect of gate
  - i.e. by increasing C_{ox} (reduce T_{ox} and/or increase ε_{ox})
- But there's another problem - leakage paths deep within transistor body:



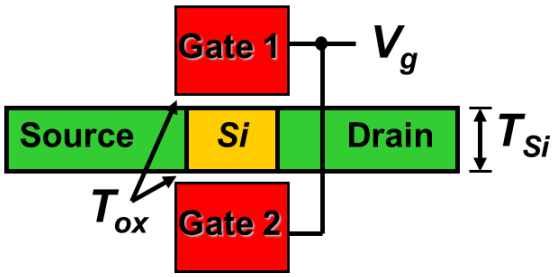
  - Gate has much weaker control in this area
  - Very difficult to turn device off

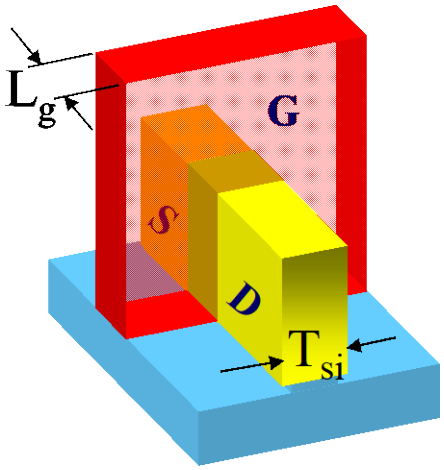


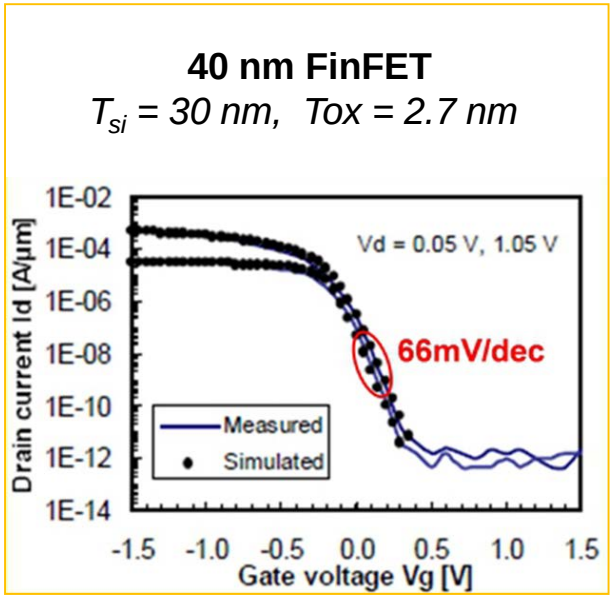
- Problem is regions in body that are as far from gate
  - allows drain to create a sub-threshold channel
- Need to completely re-think geometry of MOSFET

FinFET

- Maintain gate control by creating a narrow channel surrounded on all sides by the gate







- All portions of channel are very close to gate
  - gate maintains control of channel
  - good threshold control and sub-threshold slope
- Intel introduced FinFET into 22nm process (2012)