EE 471: Transport Phenomena in Solid State Devices

Spring 2018

Lecture 9
CMOS Digital Circuits

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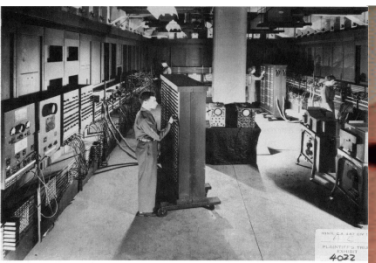
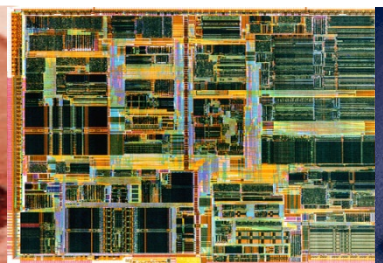
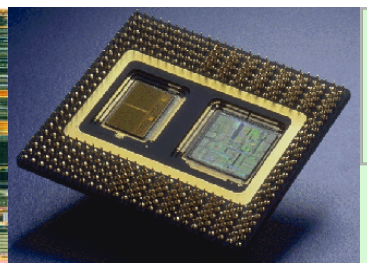
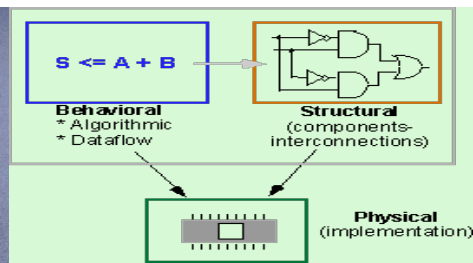
Adapted from Modern Semiconductor Devices for Integrated Circuits, Chenming Hu, 2010



CMOS Power Supply Voltages

- V_{SS} ≈ negative rail ≈ GND ≈ 0 V
- In 1980's, positive rail V_{DD} = 5V
- V_{DD} has decreased in modern processes
  - Smaller transistors require increased gate oxide capacitance C_{ox} to provide necessary current drive
  - achieved through use of thinner gate oxide ~ 2nm
  - High V_{DD} would break down gate oxide (destructively)
  - Lower V_{DD} also saves power

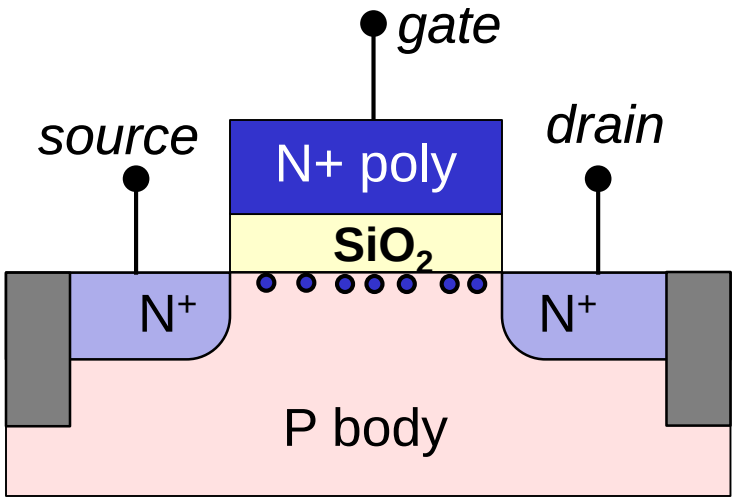
Process: 0.35μ ⇨ 0.25μ ⇨ 180nm ⇨ 130nm ⇨ 90nm ⇨ 65nm

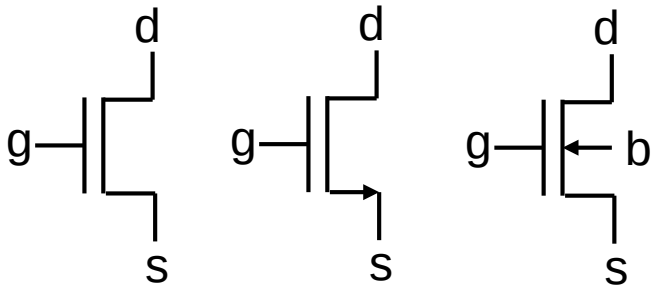
VDD: 3.3V ⇨ 2.5V ⇨ 1.8V ⇨ 1.5V ⇨ 1.2V ⇨ 1.0V ⇨ ??

- In CMOS digital circuits, conventionally define:
  - GND ≡ logical '0'
  - V_{DD} ≡ logical '1'

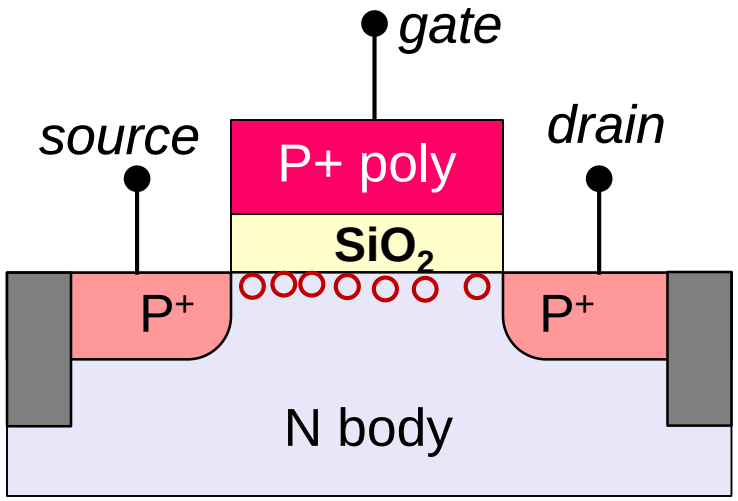
CMOS Logic Transistors

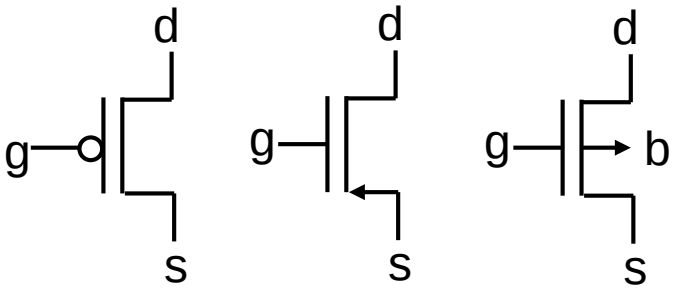
NFET or NMOS transistor





PFET or PMOS transistor

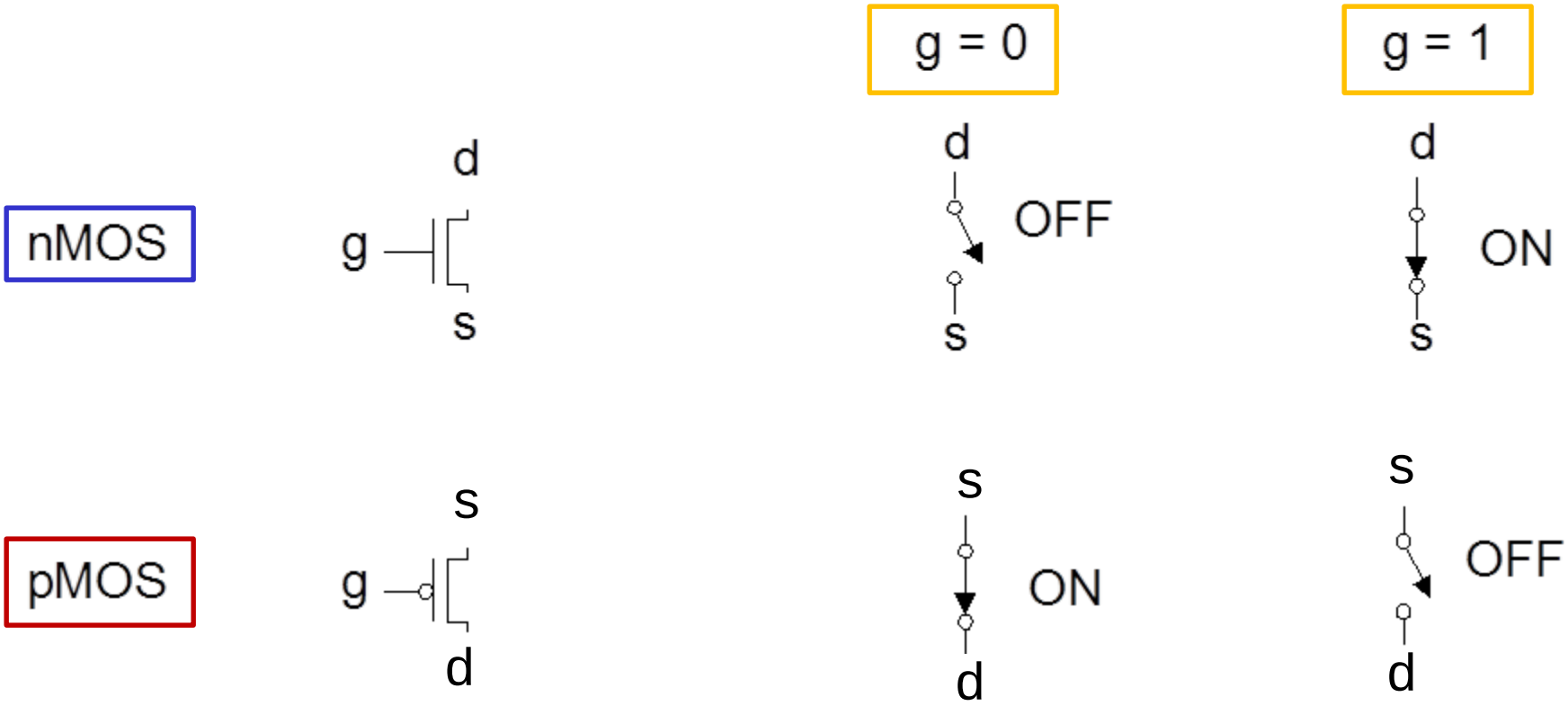




- P body normally connected to most negative voltage (0V, gnd)
- N body normally connected to most positive voltage (V_{DD})
- Both are enhancement devices with $|V_t| \approx 20\ to\ 30\%\ of\ V_{DD}$

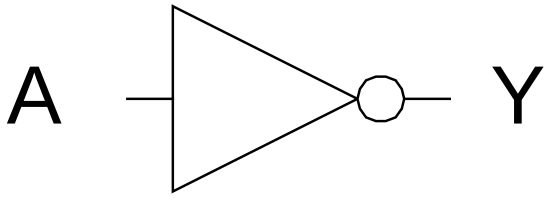
Transistors as Switches

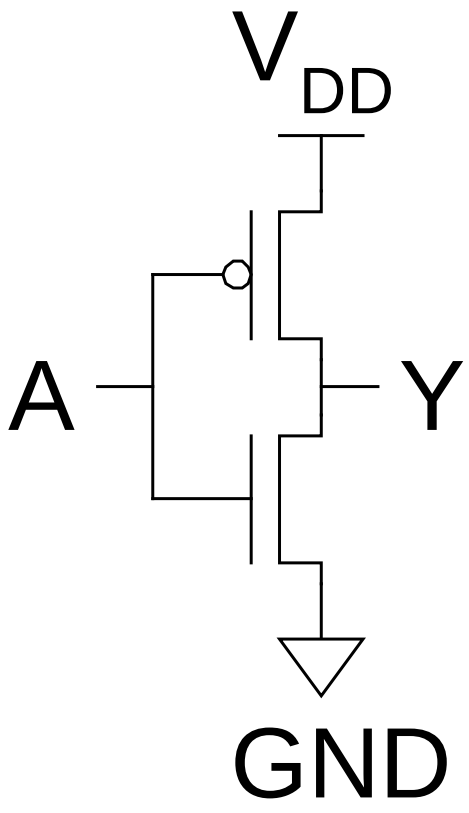
- In simplest model, we can view MOS transistors as electrically controlled switches
- Voltage at gate controls path from source to drain



CMOS Inverter

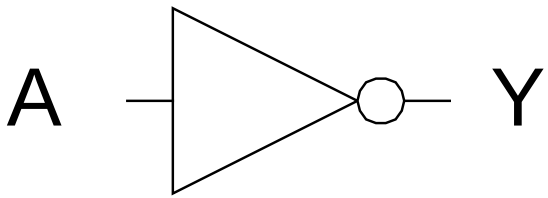
A	Y
0	
1	

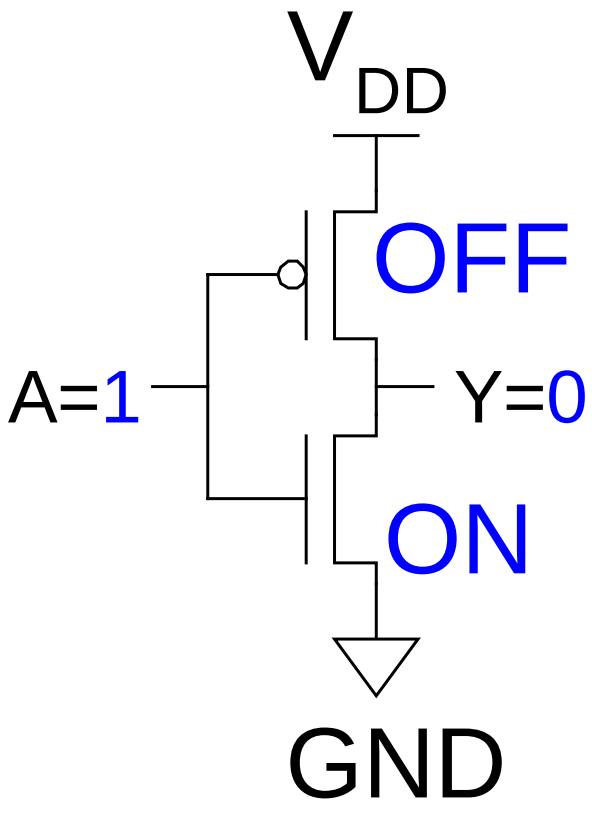




CMOS Inverter

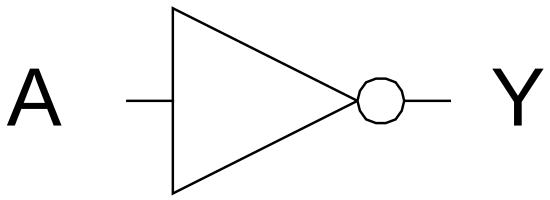
A	Y
0	
1	**0**

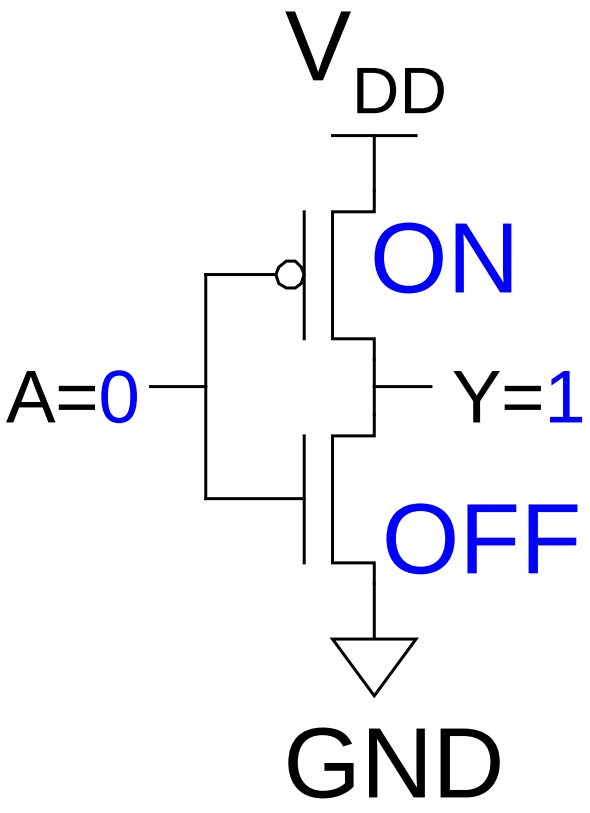




CMOS Inverter

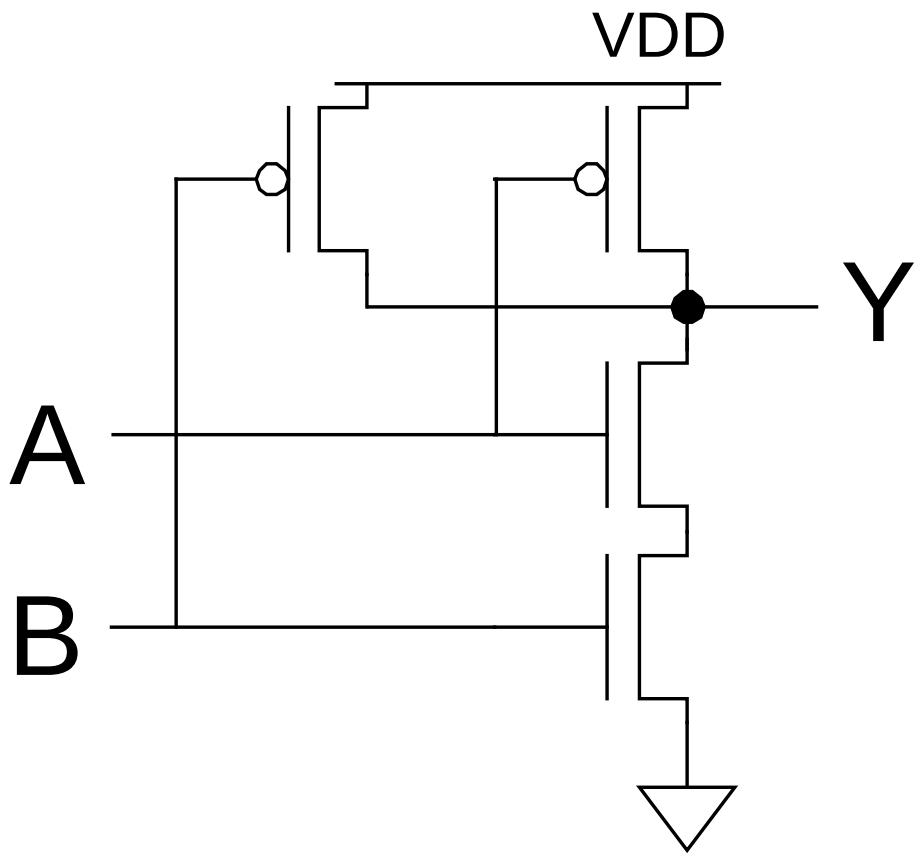
A	Y
0	**1**
1	0





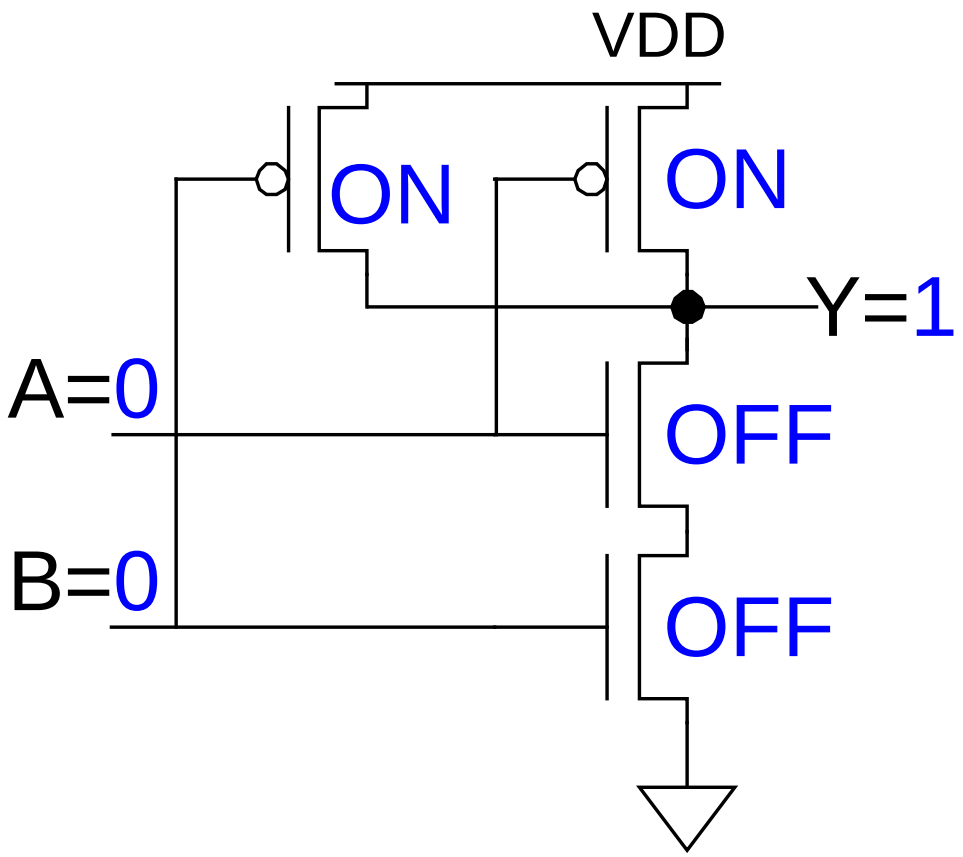
CMOS 2-input NAND Gate

A	B	Y
0	0	
0	1	
1	0	
1	1	



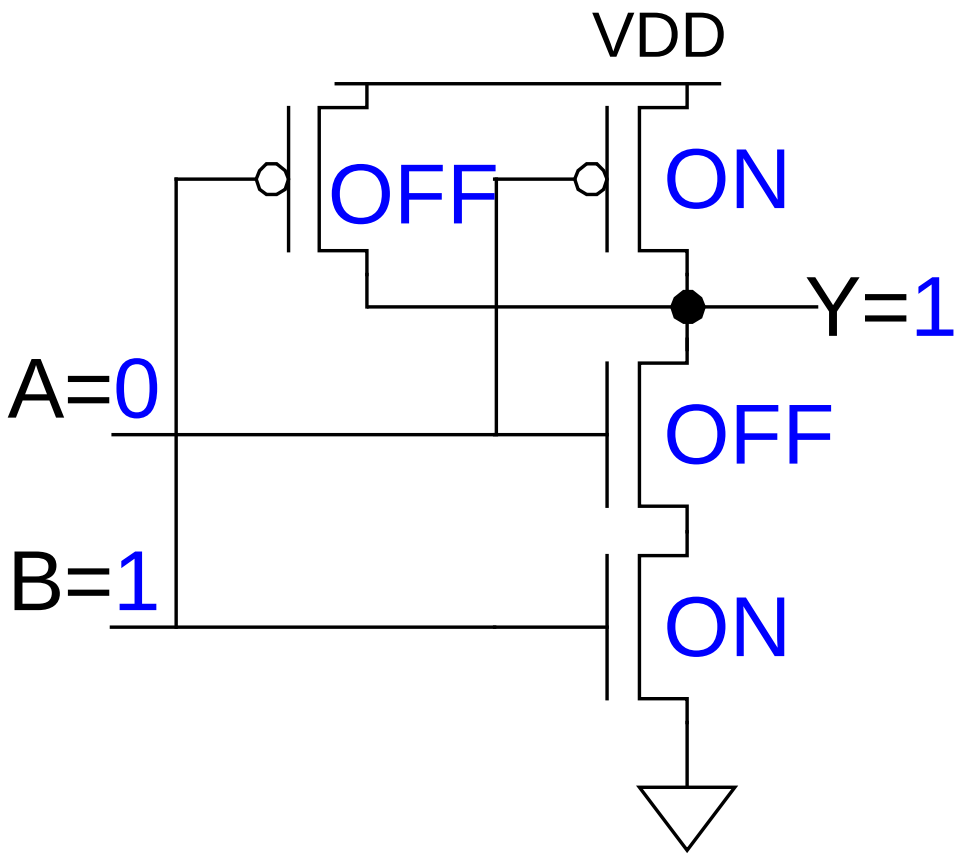
CMOS 2-input NAND Gate

A	B	Y
0	**0**	**1**
0	1	
1	0	
1	1	



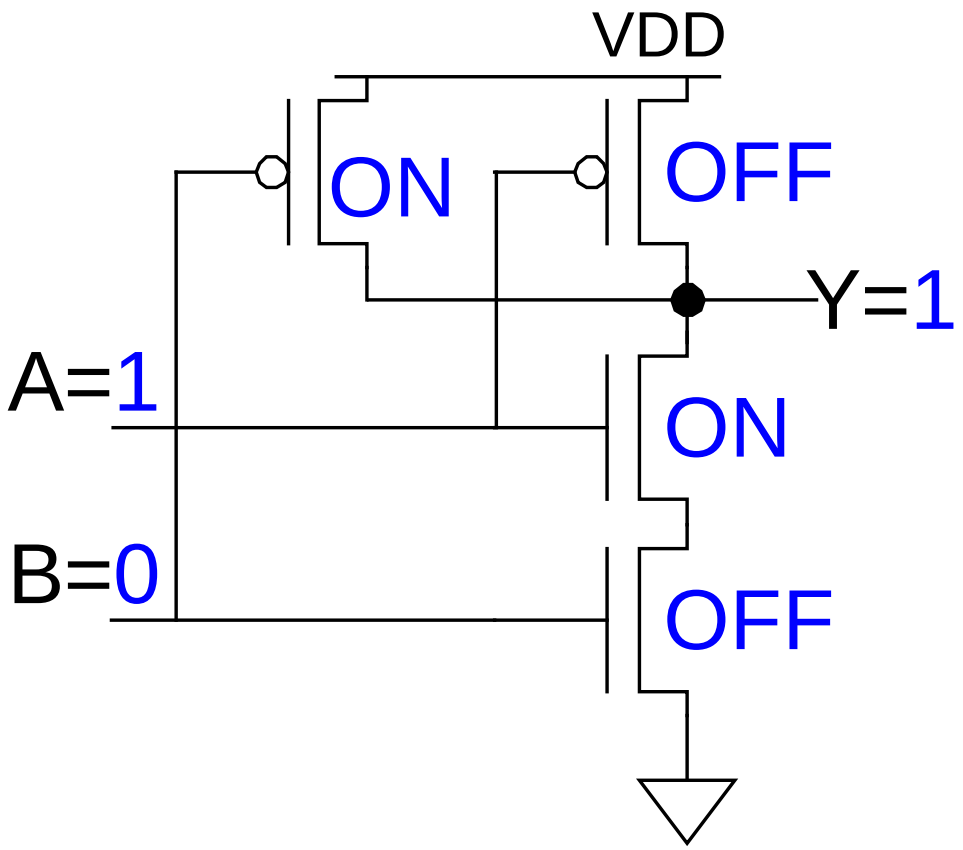
CMOS 2-input NAND Gate

A	B	Y
0	0	1
0	**1**	**1**
1	0	
1	1	



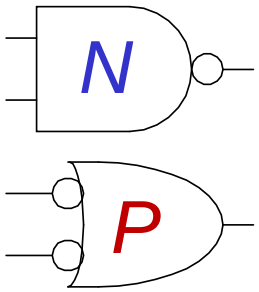
CMOS 2-input NAND Gate

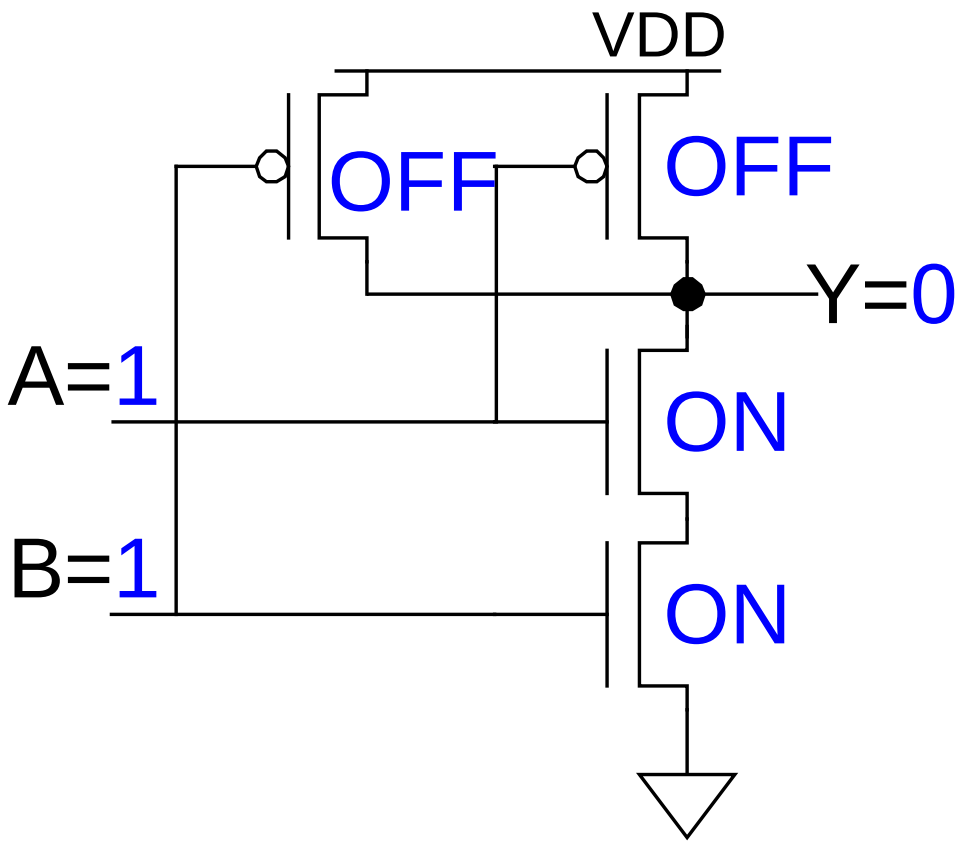
A	B	Y
0	0	1
0	1	1
1	**0**	**1**
1	1	



CMOS 2-input NAND Gate

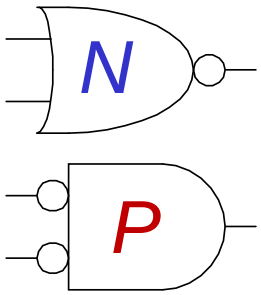
A	B	Y
0	0	1
0	1	1
1	0	1
1	**1**	**0**

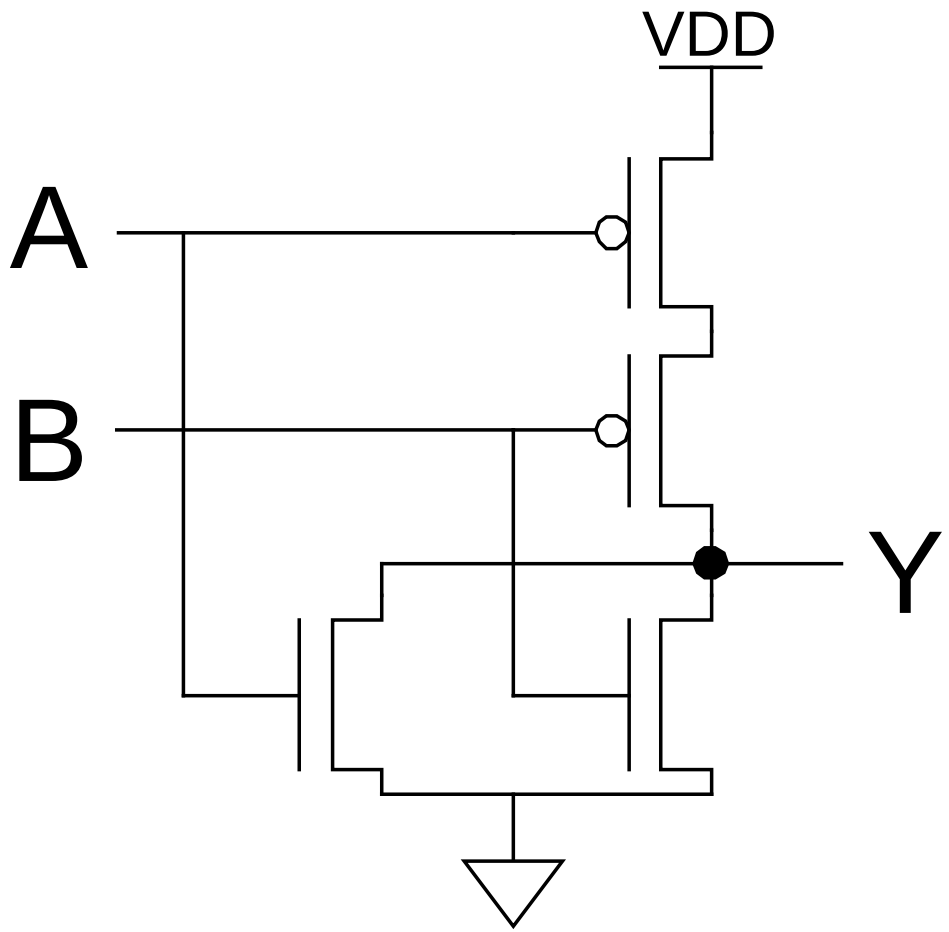




CMOS 2-input NOR Gate

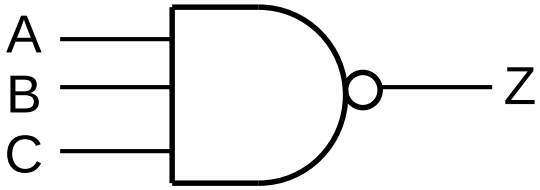
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0





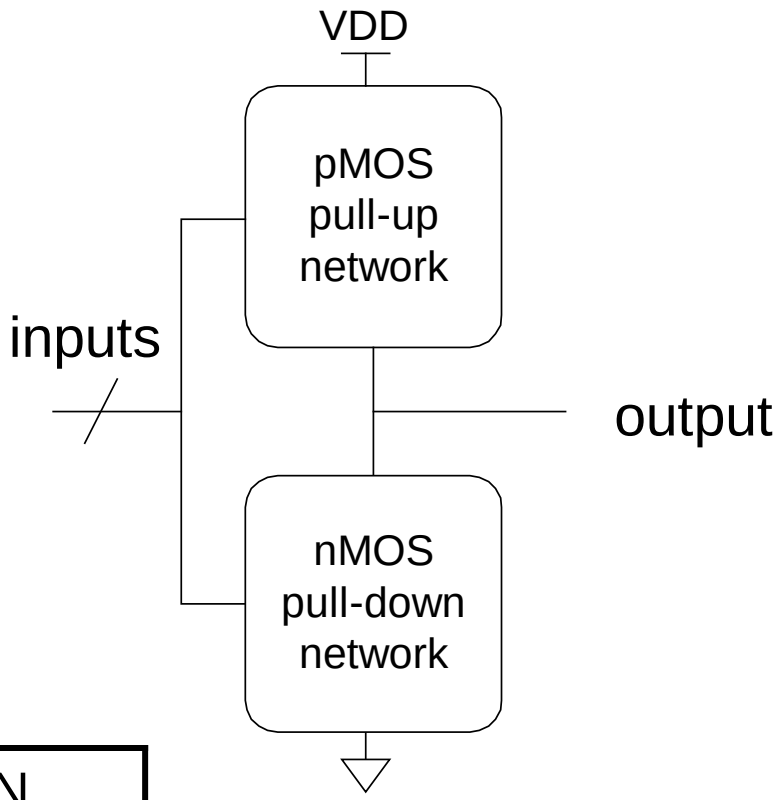
CMOS Gate Design

- Draw the transistor level schematic of a 3-input CMOS NAND gate:



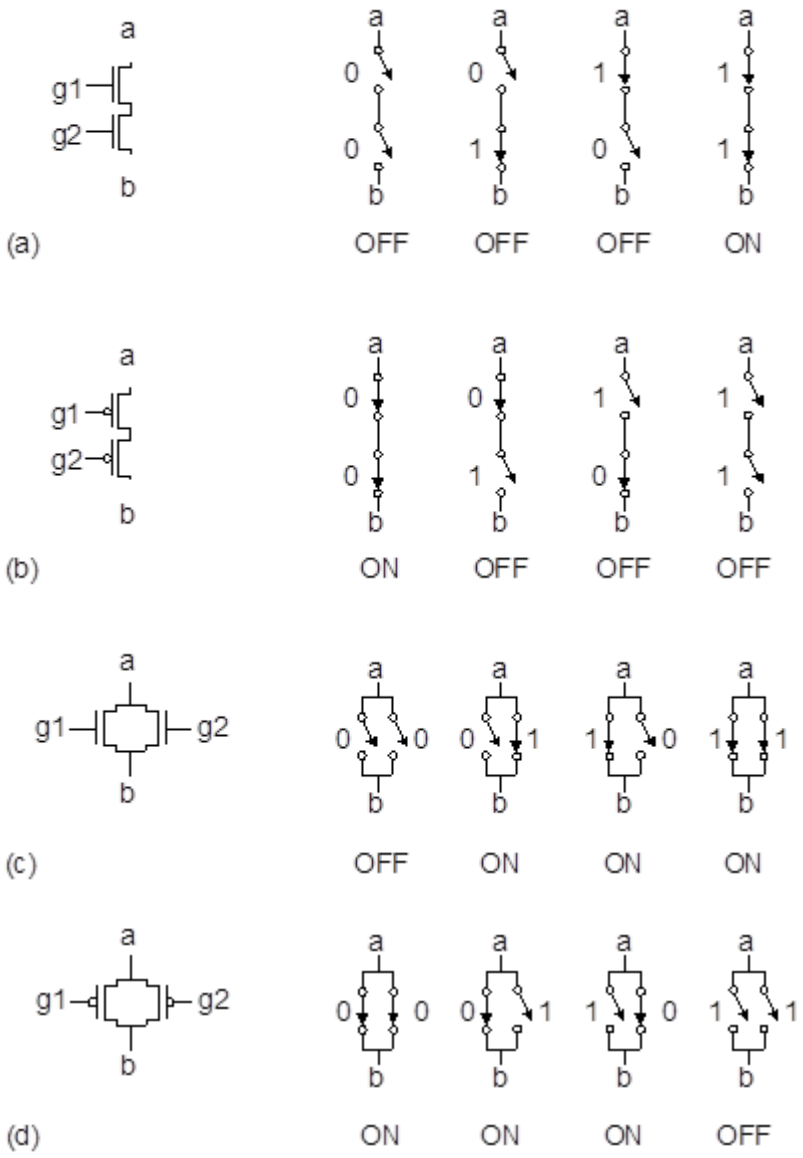
Complementary CMOS Gates

- nMOS pull-down network
- pMOS pull-up network
- static combinational CMOS logic



	Pull-up OFF	Pull-up ON
Pull-down OFF	Z (float)	**1**
Pull-down ON	**0**	X (crowbar)

Series & Parallel Conduction Paths

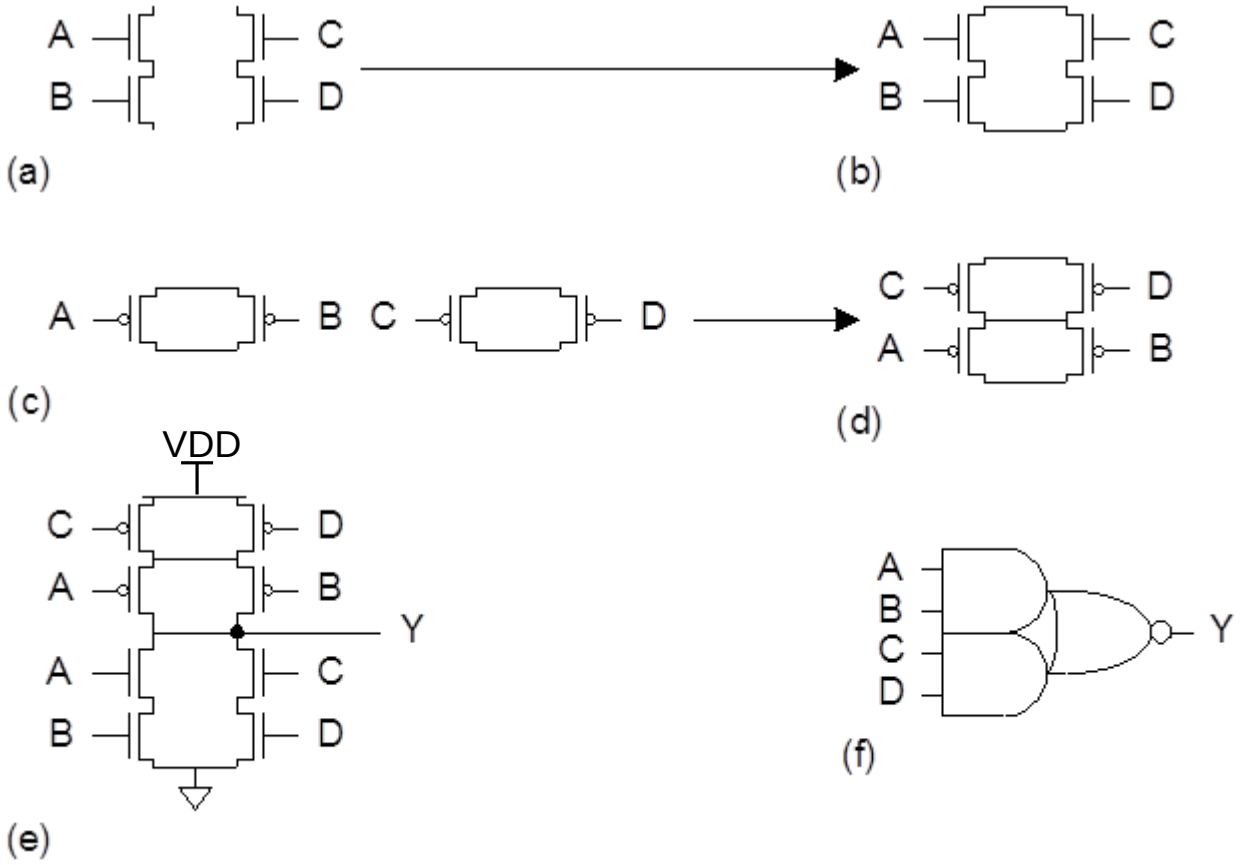


- nMOS: 1 = ON
- pMOS: 0 = ON
- Series: both must be ON
- Parallel: either can be ON

- To ensure that gate is always driven to 0 or 1:
- Pull-up network must be topological complement of pull-down network
  - parallel ⇨ series
  - series ⇨ parallel

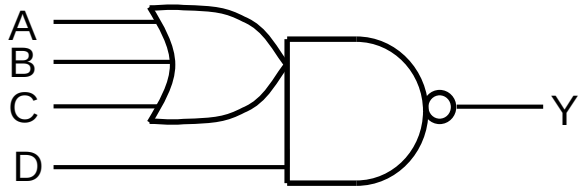
Compound Gates

- We can generate any inverting combinatorial function with a network of series and parallel nMOS transistors and a complementary network of pMOS transistors
- e.g., $Y = \overline{A.B + C.D}$ *and-or-invert gate*: AOI22



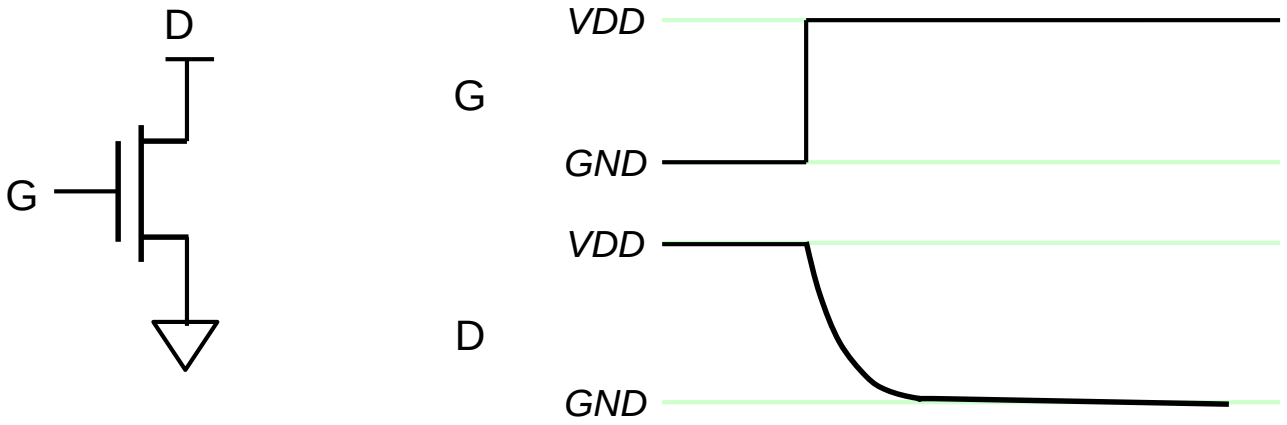
Example: O3AI

- $Y = \overline{(A + B + C).D}$



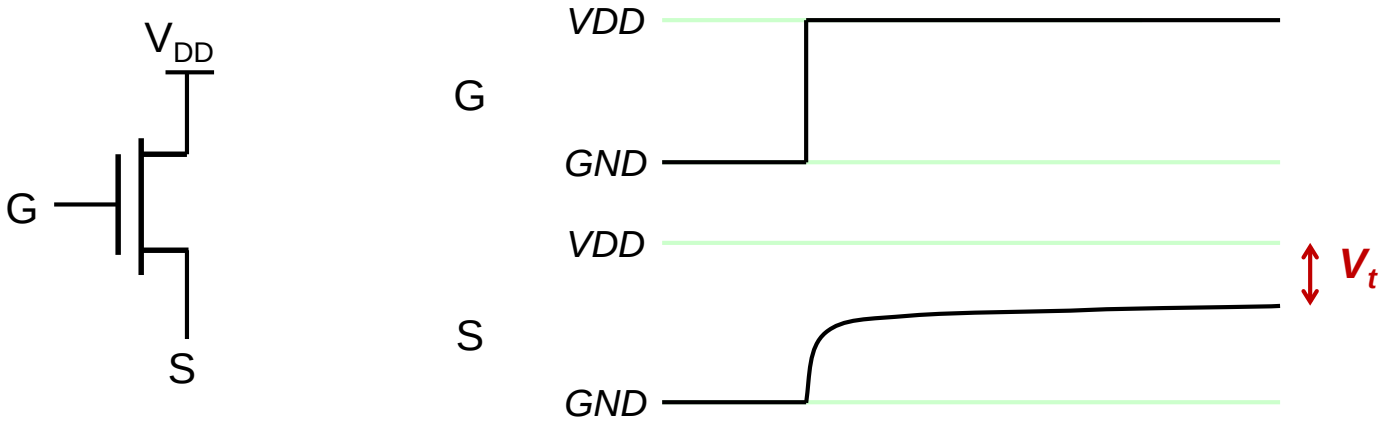
Signal Strength

- In a complementary gate, nMOS transistors are always used to pull down to GND and pMOS are always used to pull up to V_{DD}



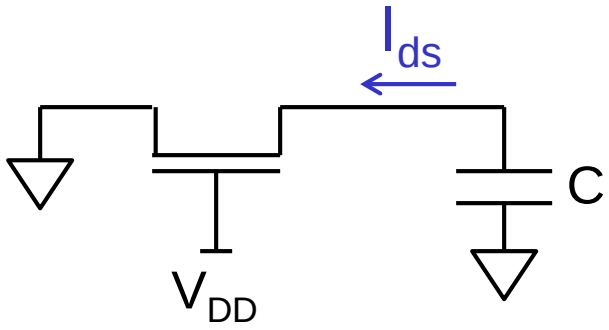
- Once gate goes high, $V_g - V_s = V_{DD} > V_{th}$
- Transistor stays on as drain is pulled all way down to GND
- Could we use an nMOS transistor to pull-up to V_{DD}?

Pulling up with an nMOS



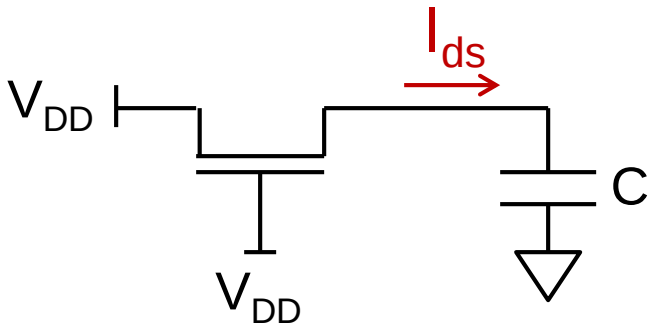
- In this configuration, source voltage is changing
- As $V_g - V_s$ approaches V_{th}, transistor starts to turn off
- Weak conduction leads to degraded final value
  - never reaches V_{DD}. V_s asymptotes towards $V_{DD} - V_t$
- Furthermore, body effect increases V_t when $V_{sb} > 0$
- As a switch, we say nMOS drives (passes) a strong 0 but a degraded or weak 1
  - Similarly pMOS drives a strong 1 but a degraded or weak 0

Degraded Time Constant



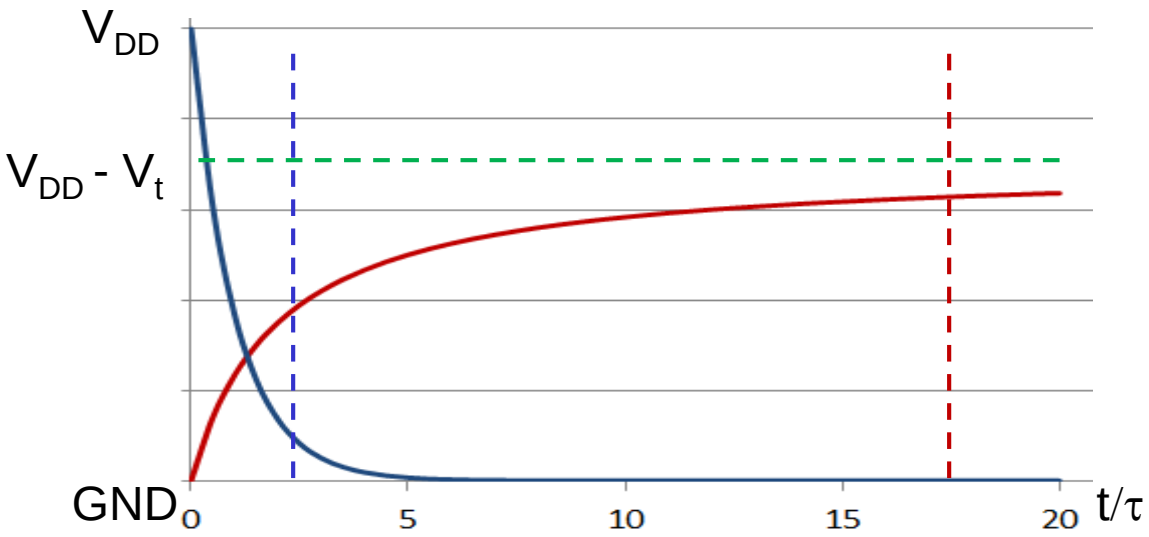
pull-down device is in linear (mostly):

$I_{ds} \alpha V_d$



pull-up device is in saturation:

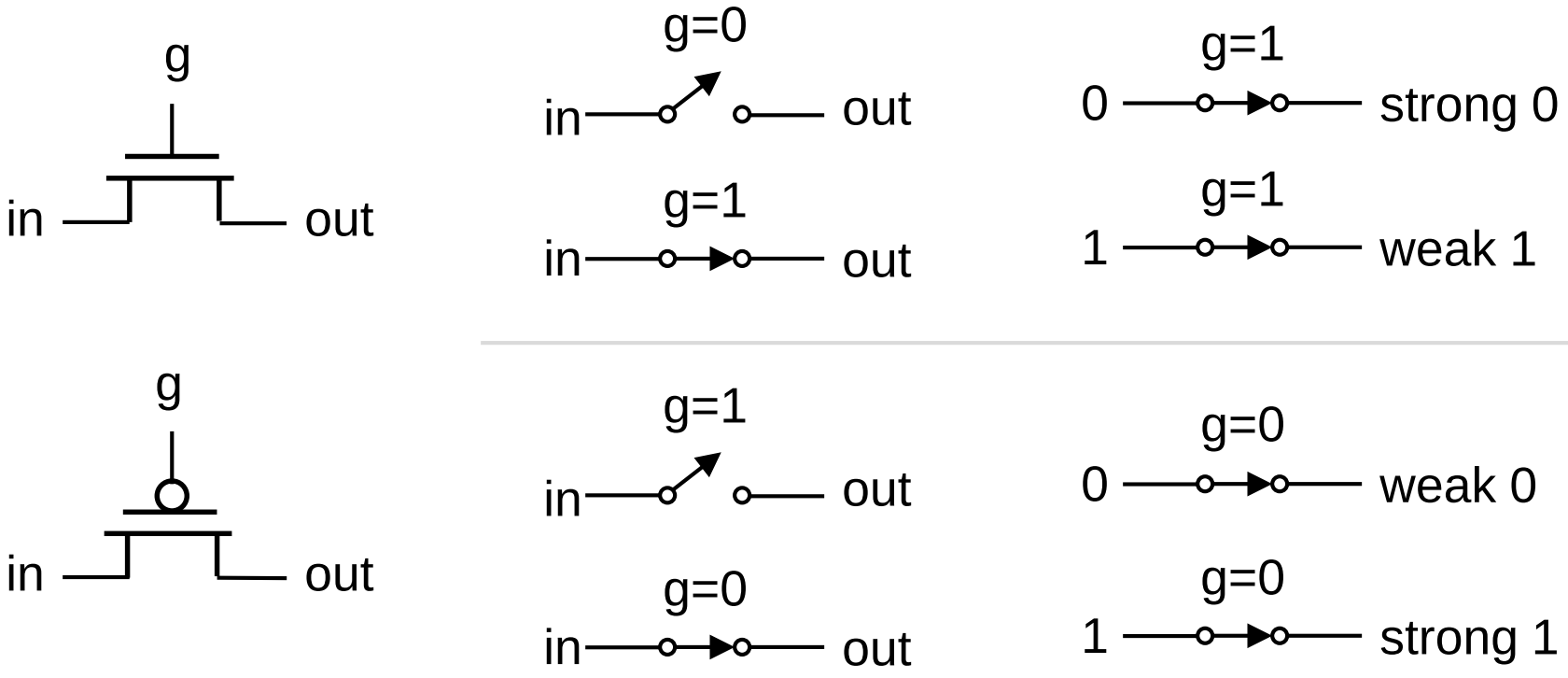
$I_{ds} \alpha ((V_{DD} - V_t) - V_s)^2$



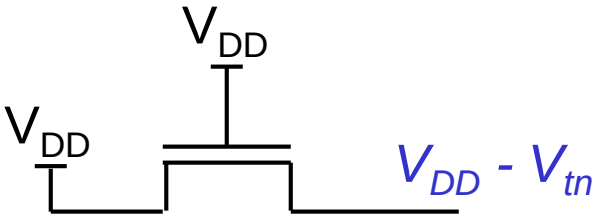
Pull-up time constant (to 90% final value) can be 6x pull-down time constant!

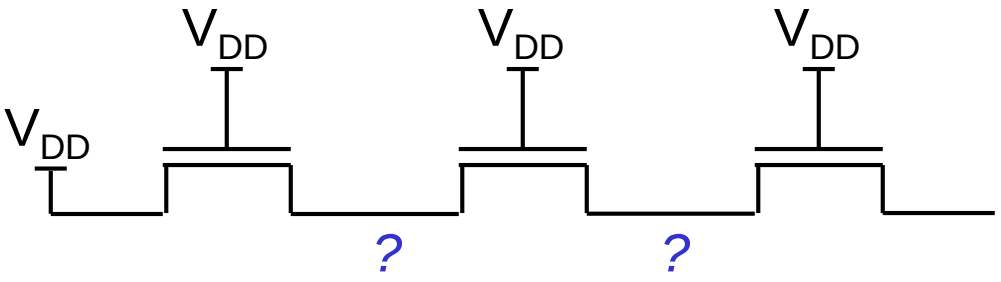
Pass Transistors

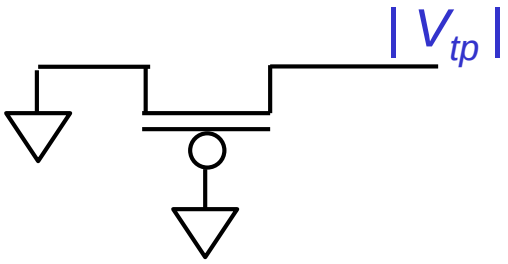
- So far, we have used nMOS to switch (drive) output to GND and pMOS to switch (drive) output to VDD in response to various input signals
- We can also used MOS transistors to switch the input signals themselves

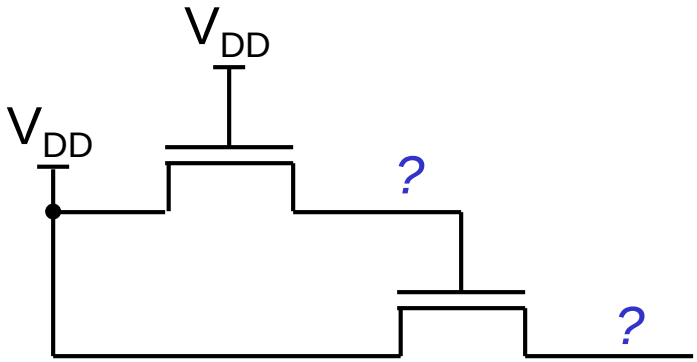


Cascaded Pass Transistors



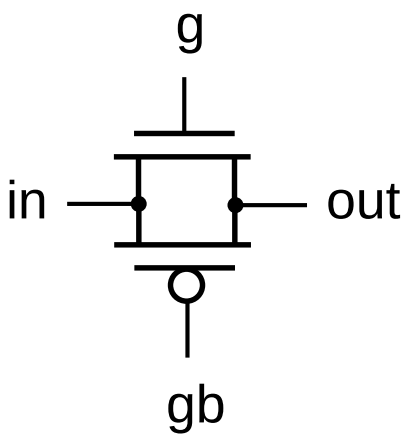


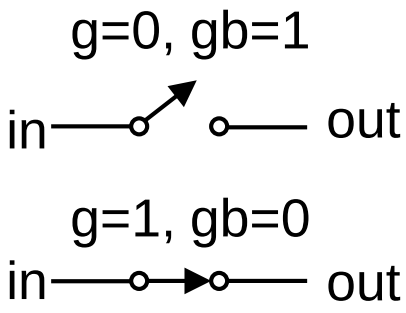


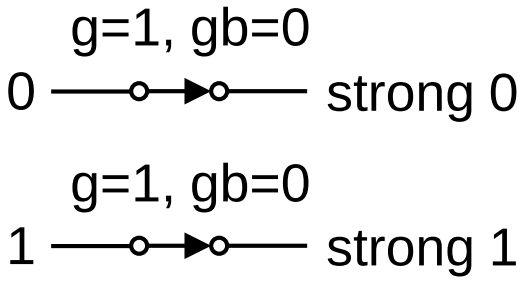


Transmission Gate

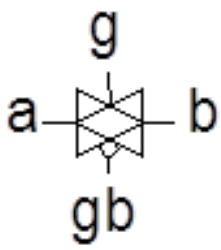
- Transmission gate is a pMOS and nMOS pass transistor in parallel
- Passes a strong 0 and a strong 1

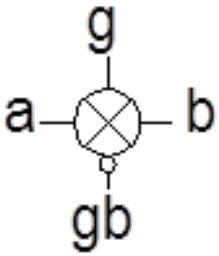


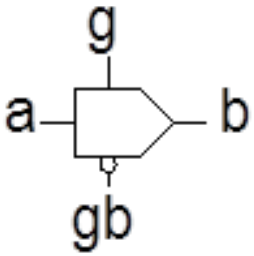




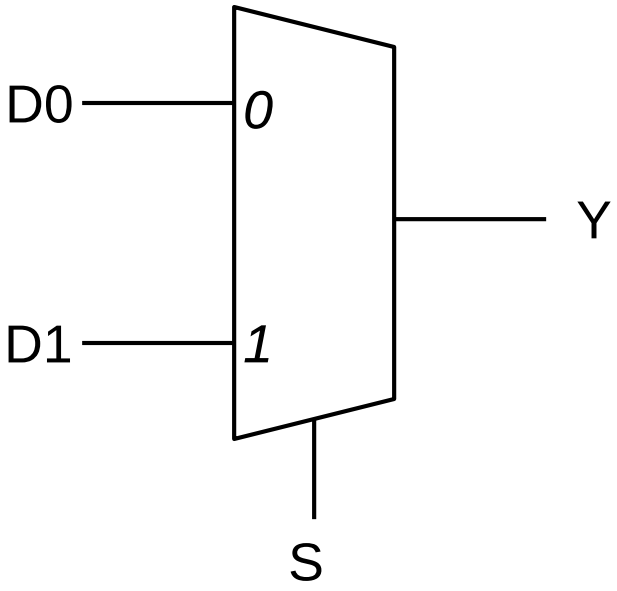
- Common schematic symbols:







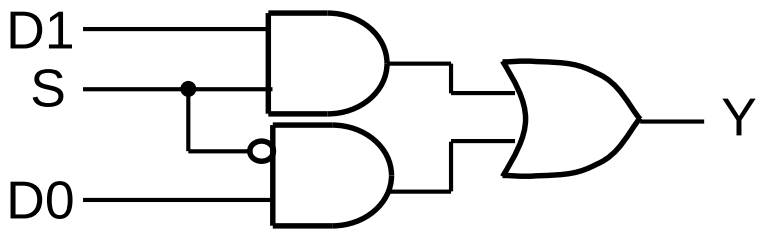
2:1 Multiplexer



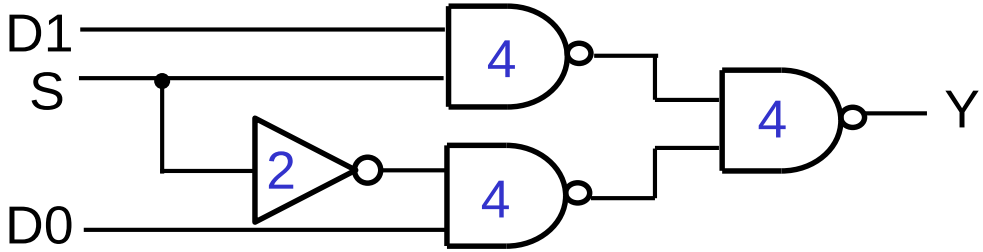
S	D1	D0	Y
0	X	0	0
0	X	1	1
1	0	X	0
1	1	X	1

Mux Design using Standard Logic Gates

- $Y = \overline{S}.D0 + S.D1$

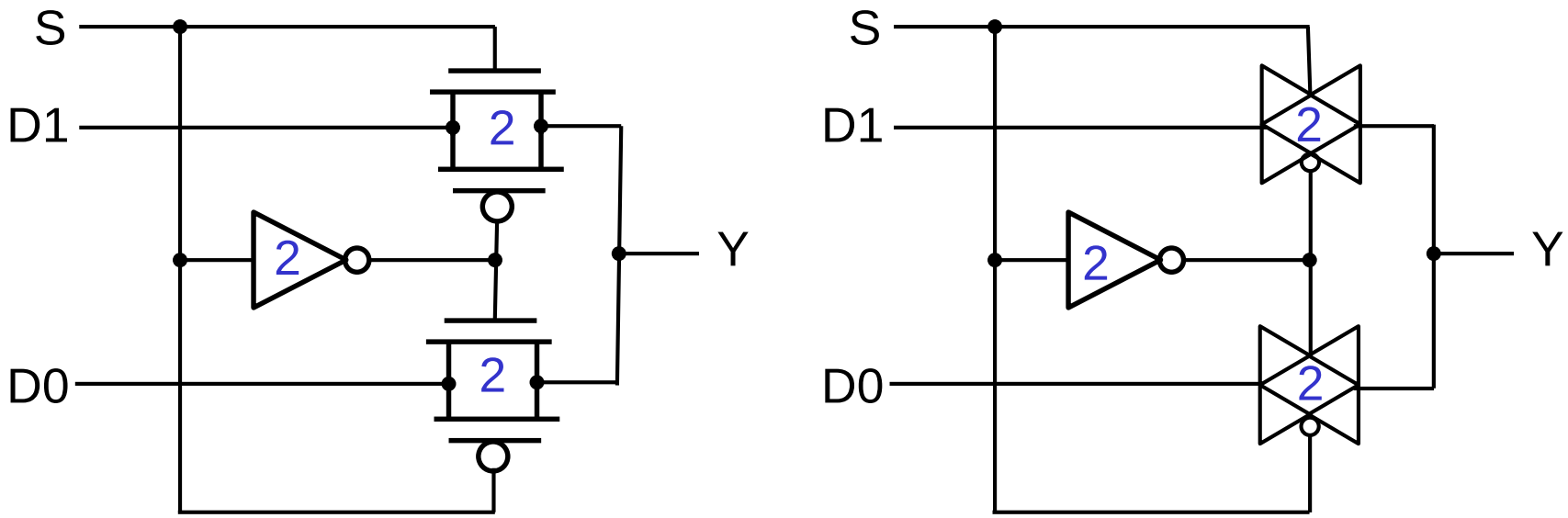


using complimentary inverting gates



- Requires 14 transistors

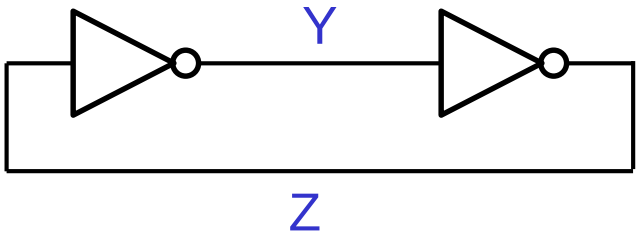
Mux Design using Transmission Gates



- Requires only 6 transistors
- Use with caution: non-restored logic
- Long chains of transmission gates lead to long delays and degraded levels

Storage Elements

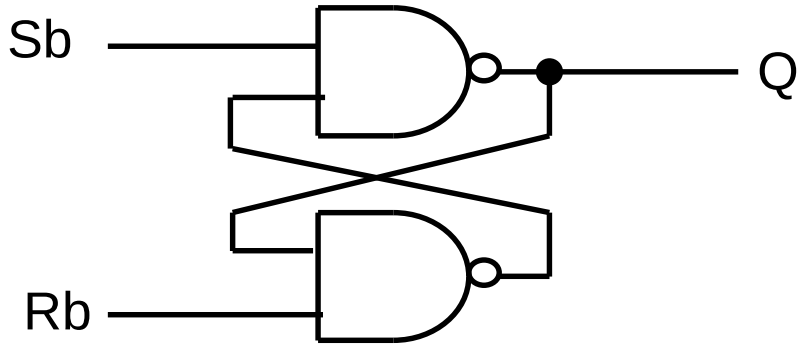
- Basic static storage element is cross-coupled inverter



- Positive feedback drives circuit into one of two stable states
- Either: (Y=1, Z=0) *OR* (Y=0, Z=1)
- Circuit will hold state indefinitely
  - restoring effect of digital logic eliminates degradation of stored levels over time
- How do we change the state?

RS Latch

- Simple “writable” storage element



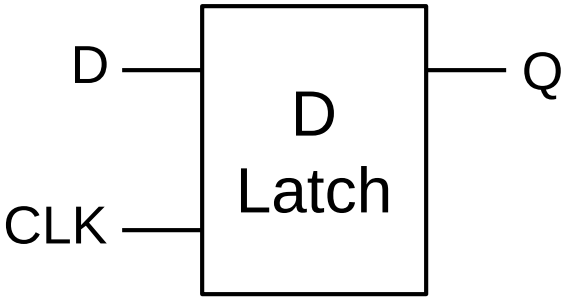
Rb	Sb	Q
0	1	0
1	0	1
1	1	*no change*
0	0	*illegal*

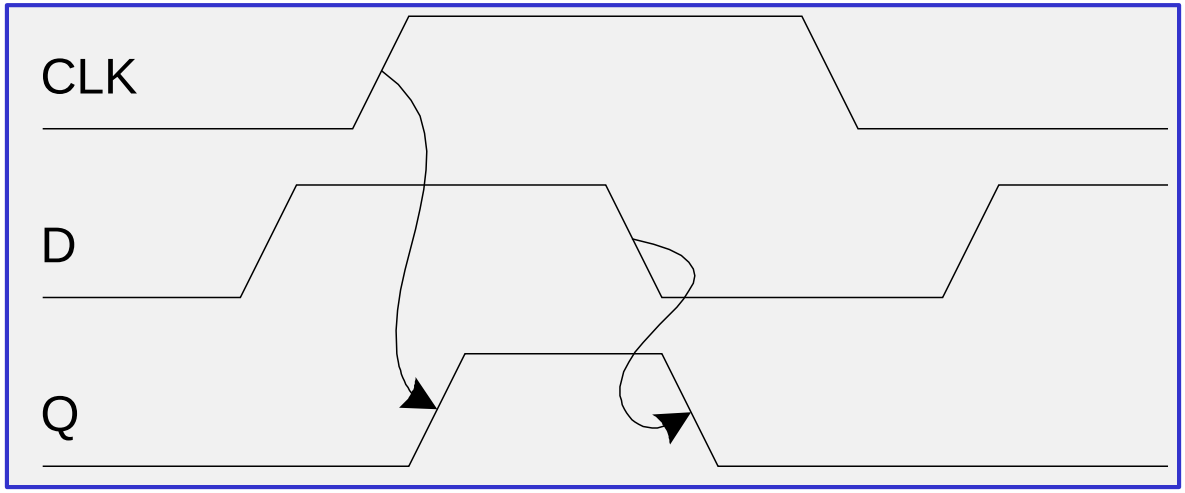
- Normally, Sb and Rb are both 1
- When Sb=0, Q is set to 1
- When Rb=0, Q is reset to 0

D Latch

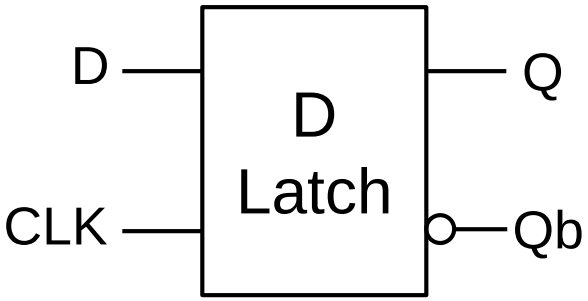
- When CLK = 1, latch is transparent
- D flows through to Q like a buffer
- When CLK = 0, the latch is opaque
- Q holds its old value independent of D
- a.k.a. transparent latch or level-sensitive latch

D	CLK	Q
0	1	0
1	1	1
0	0	*no change*
1	0	*no change*

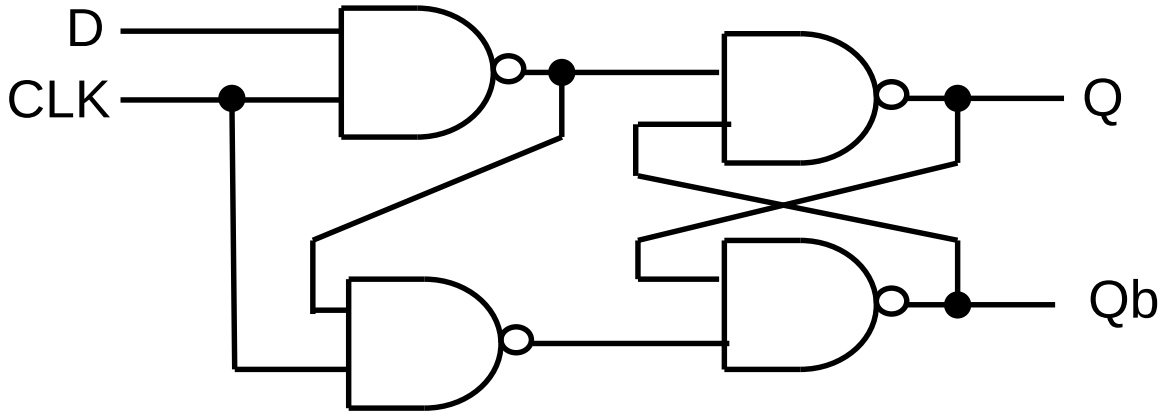




D Latch using Standard Logic Gates

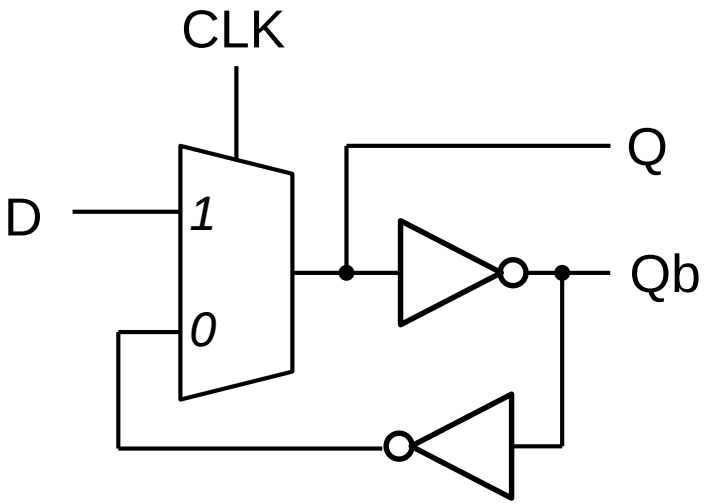


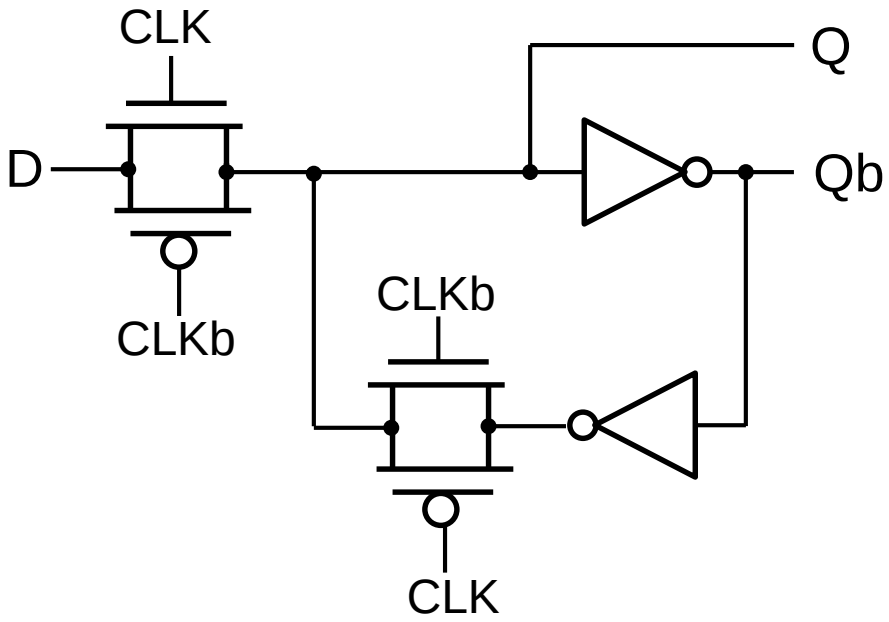
D	CLK	Q	Qb
0	1	0	1
1	1	1	0
0	0	*no change*	*no change*
1	0	*no change*	*no change*



- Uses 16 transistors
- Up to 4 gate delays (D to Q)

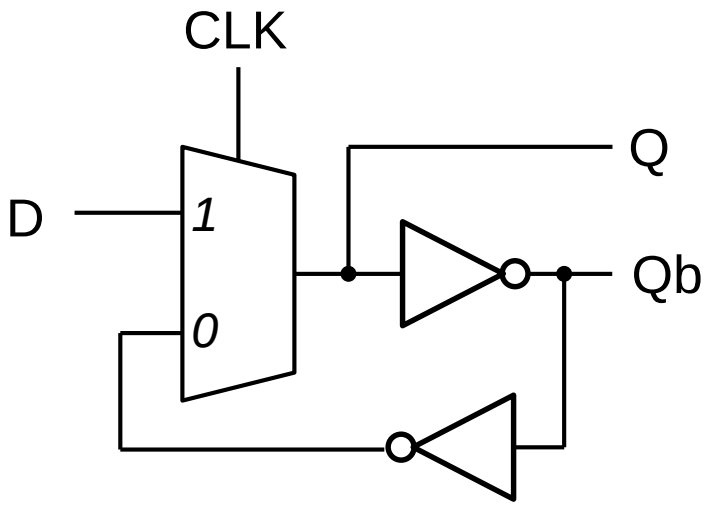
D Latch using Transmission Gate

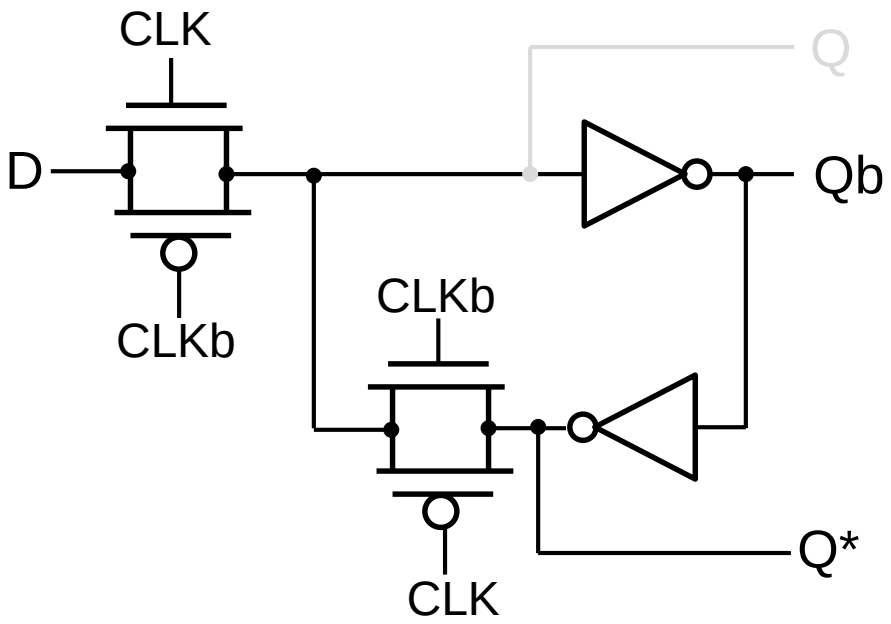




- Multiplexer chooses D or stored Q
- Uses 8 (+2) transistors
- Fast response D to Q
- Q is non-restored

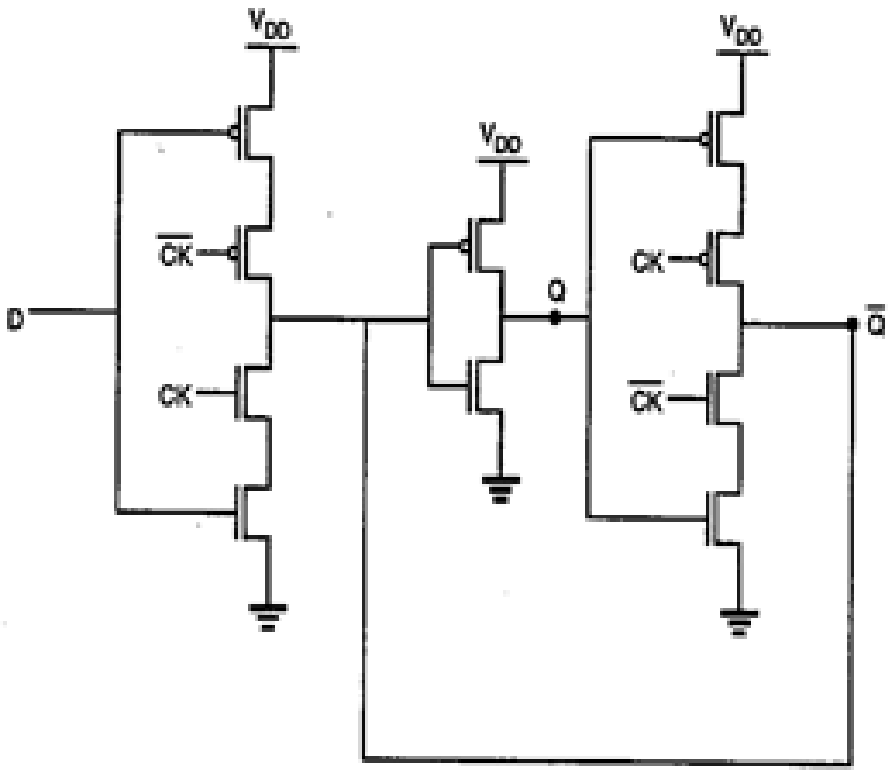
D Latch using Transmission Gate





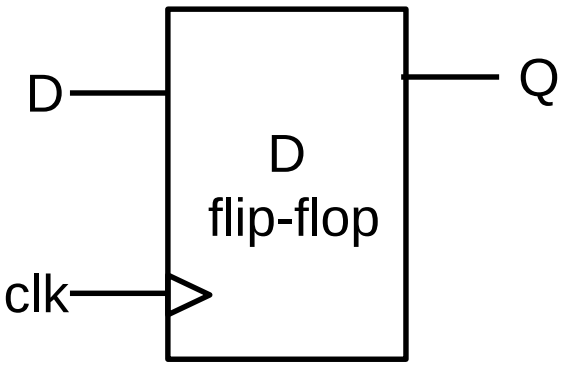
- Multiplexer chooses D or stored Q
- Uses 8 (+2) transistors
- Fast response D to Q
- Q is non-restored
- Q* is slower response, but fully restored

Alternative CMOS D Latch



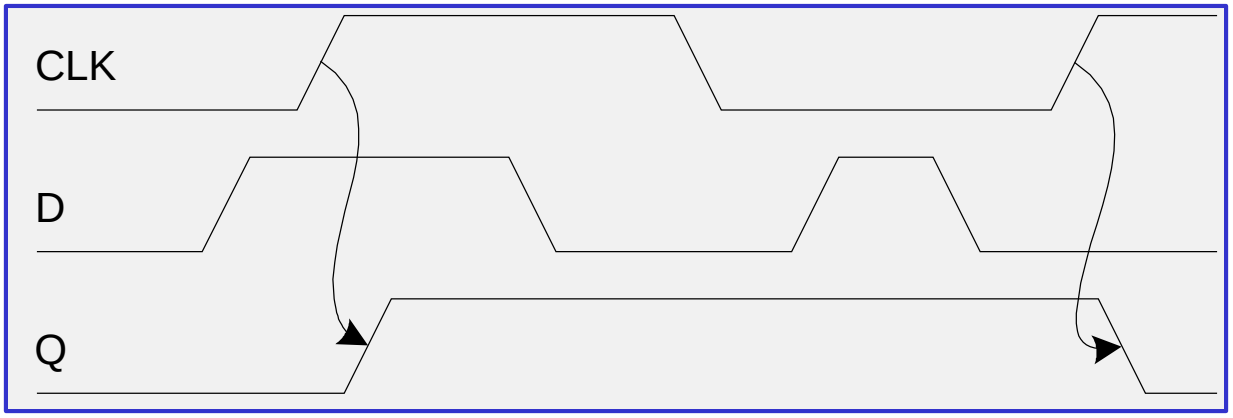
- What is happening here?

D Flip-flop



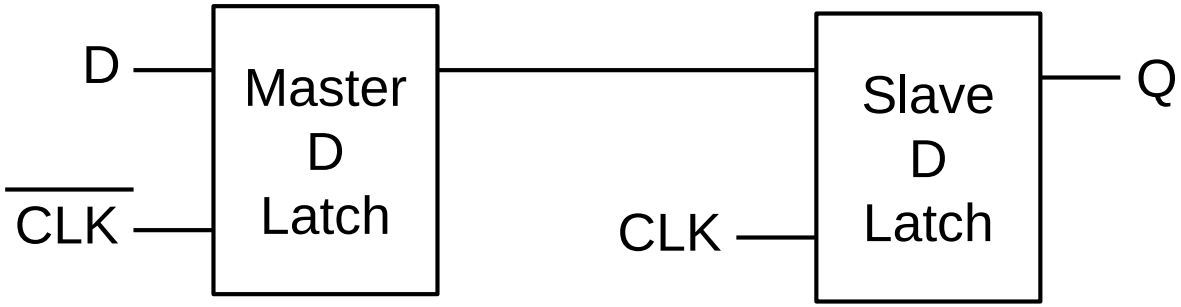
clk	D	Q
0	X	no change
1	X	no change
↑	1	1
↑	0	0

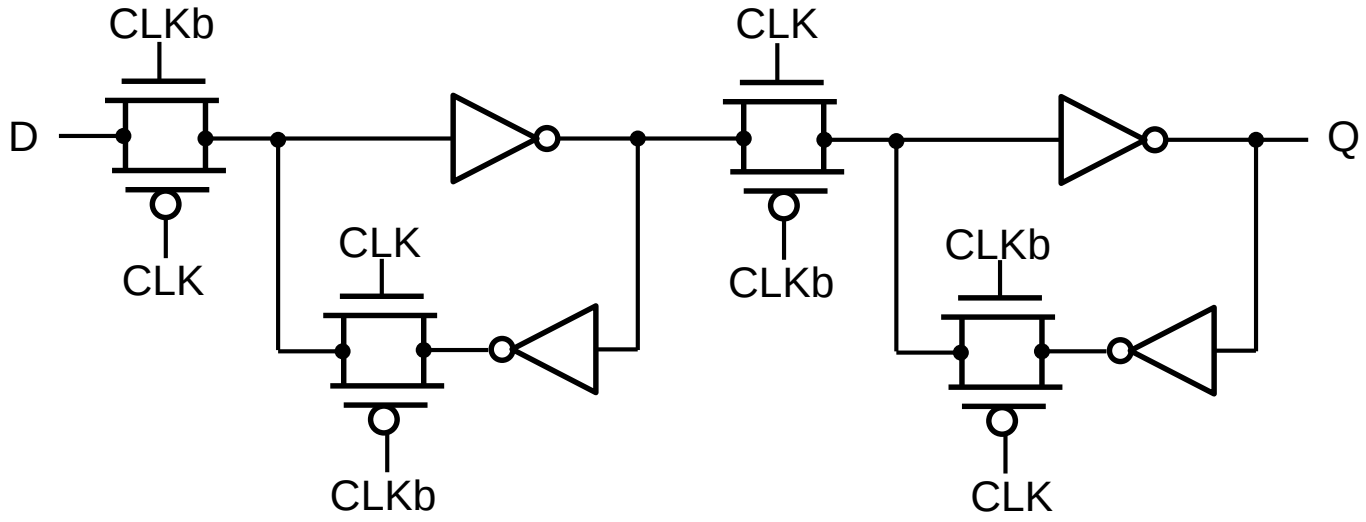
- When CLK rises, D is copied to Q
- At all other times, Q holds its value
- a.k.a. edge-triggered flip-flop, master-slave flip-flop



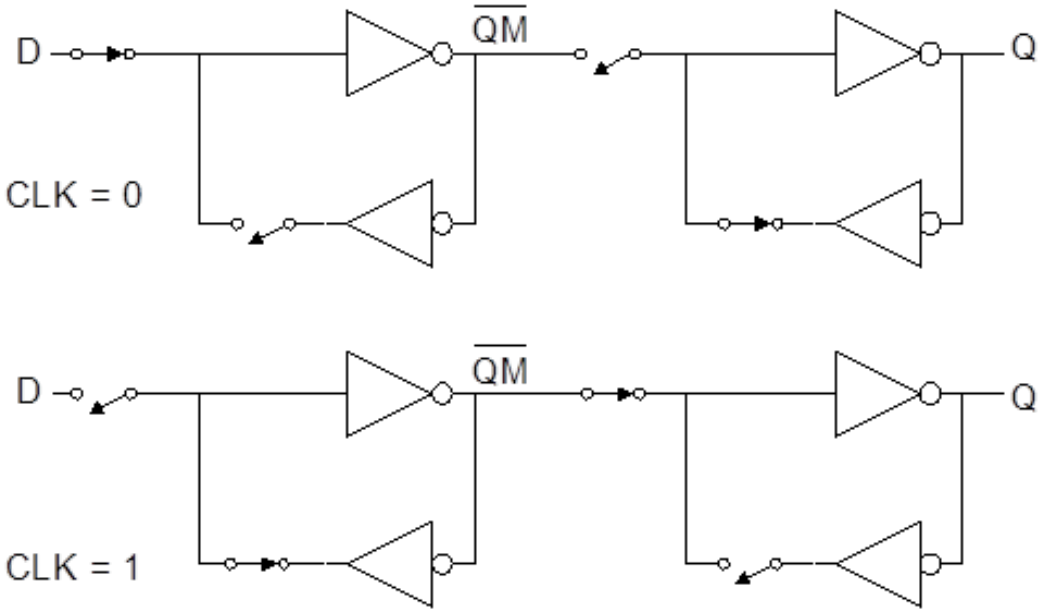
Master-Slave Latches

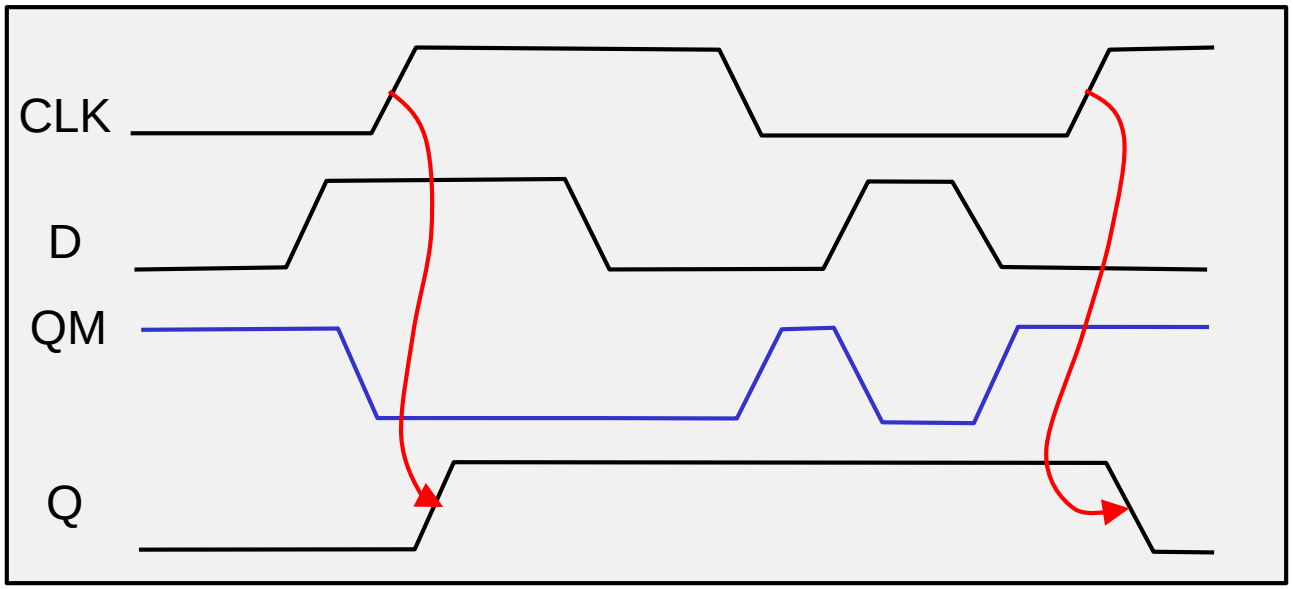
- D Flip-flop is built from two D latches



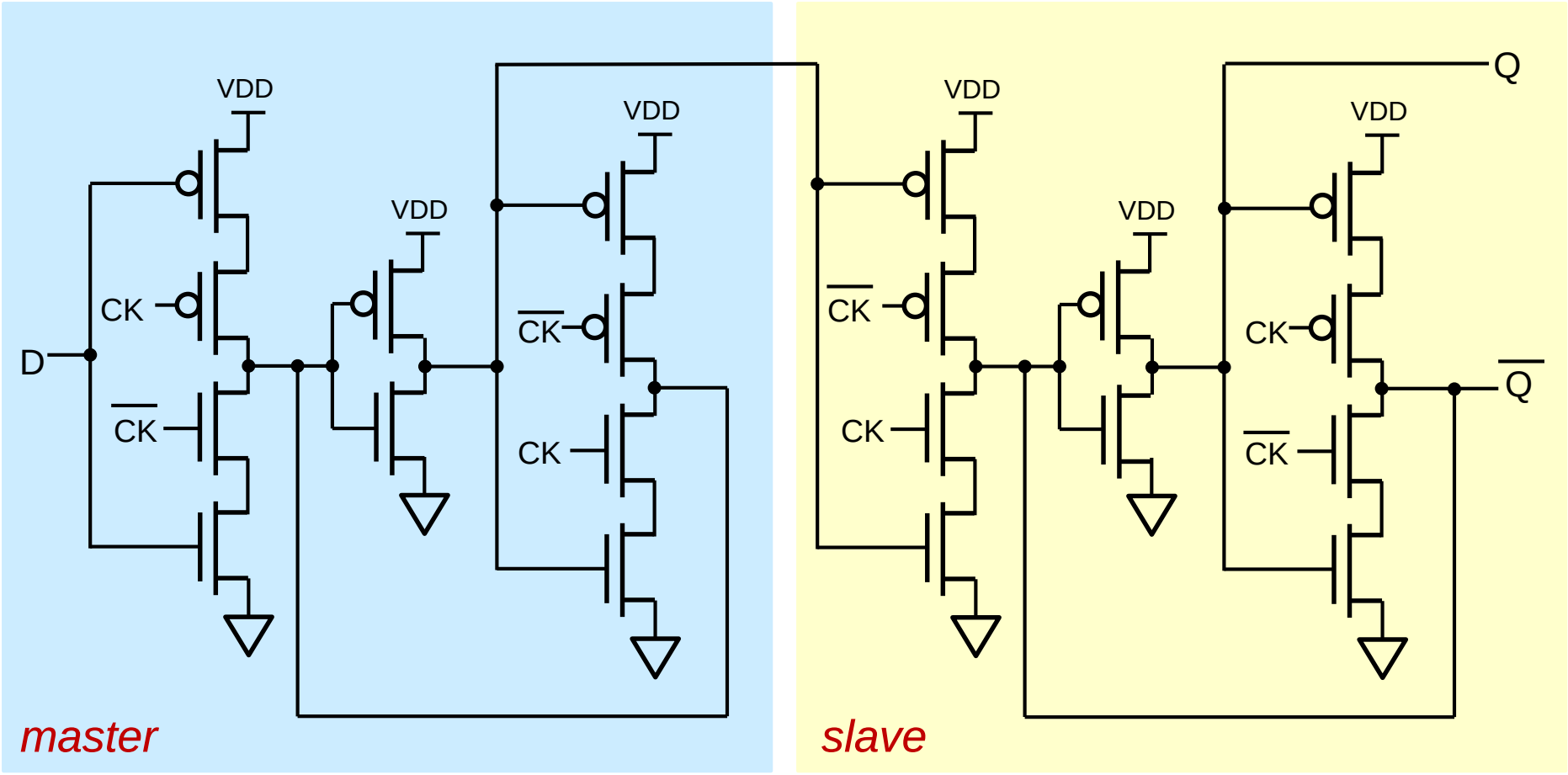


D Flip-flop Operation





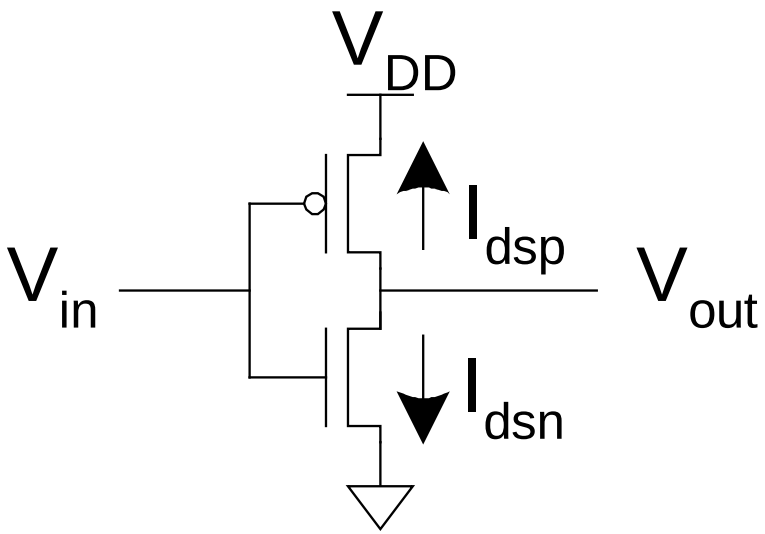
Another D-Flip-flop Implementation



DC Response: Inverter

- Digital circuits are merely analog circuits used over a constrained portion of their range
- Derive DC transfer function for static CMOS inverter
- When $V_{in} = 0 \Rightarrow V_{out} = V_{DD}$
- When $V_{in} = V_{DD} \Rightarrow V_{out} = 0$
- In between, V_{out} depends on transistor size and current
- By KCL, must settle such that

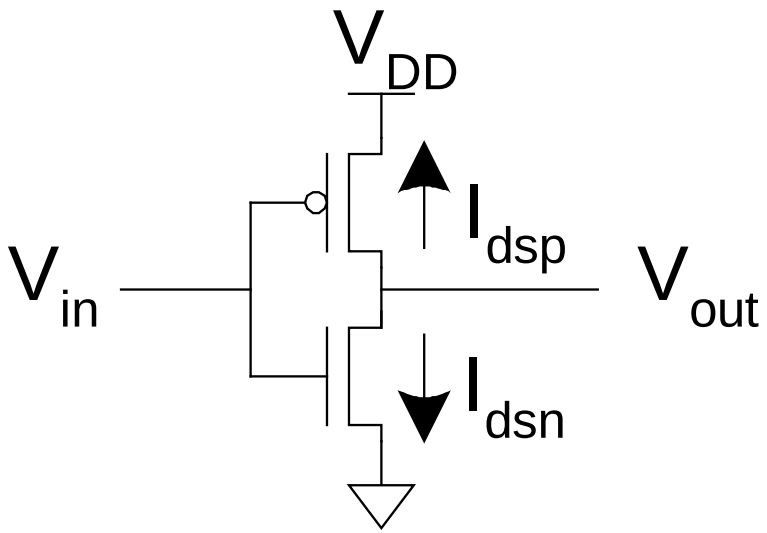
  $I_{dsn} = |I_{dsp}|$



- We could solve equations, but …
- Graphical solution gives more insight

Transistor Operation

- Current (I_{dsn}, I_{dsp}) depends on region of transistor behavior
- For what V_{in} and V_{out} are nMOS and pMOS in
- Cutoff?
- Linear?
- Saturation?

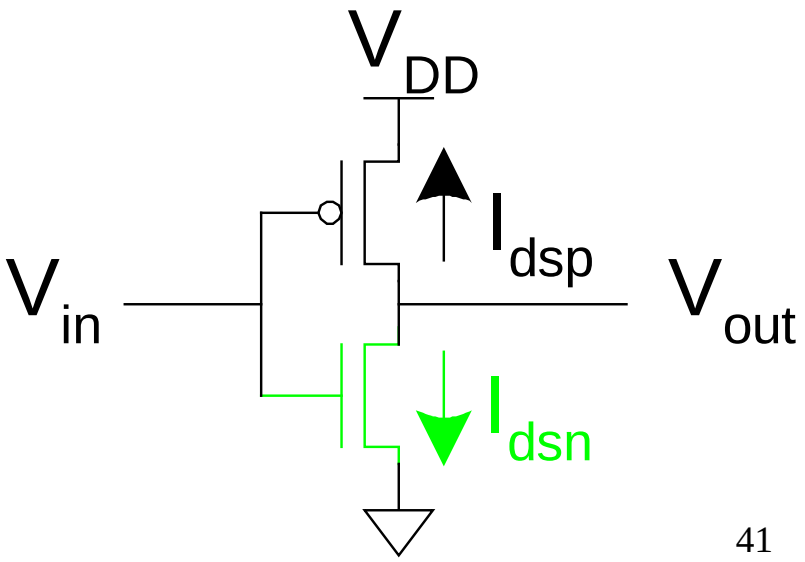


Inverter: nMOS Operation

Cutoff	Linear	Saturated
$V_{gsn} < V_{tn}$	$V_{gsn} > V_{tn}$	$V_{gsn} > V_{tn}$
$V_{in} < V_{tn}$	$V_{in} > V_{tn}$	$V_{in} > V_{tn}$
	$V_{dsn} < V_{gsn} - V_{tn}$	$V_{dsn} > V_{gsn} - V_{tn}$
	$V_{out} < V_{in} - V_{tn}$	$V_{out} > V_{in} - V_{tn}$

$V_{gsn} = V_{in}$

$V_{dsn} = V_{out}$



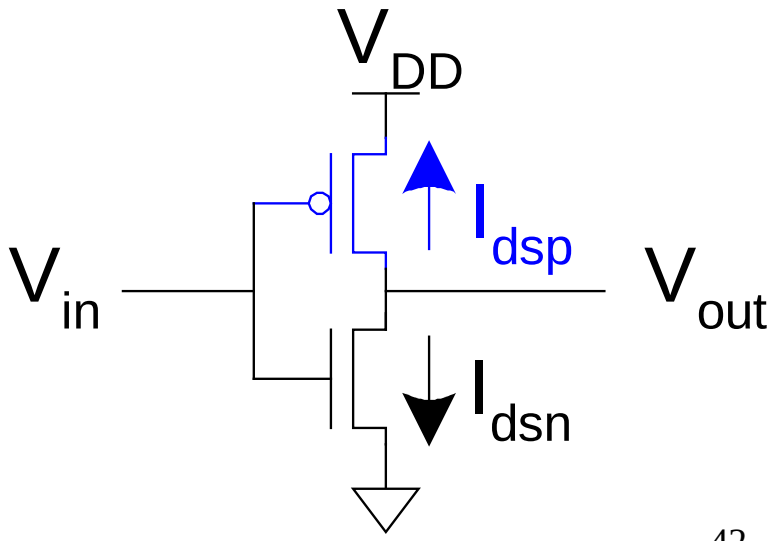
Inverter: pMOS Operation

Cutoff	Linear	Saturated
$V_{gsp} > V_{tp}$	$V_{gsp} < V_{tp}$	$V_{gsp} < V_{tp}$
$V_{in} > V_{DD} + V_{tp}$	**$V_{in} < V_{DD} + V_{tp}$**	**$V_{in} < V_{DD} + V_{tp}$**
	$V_{dsp} > V_{gsp} - V_{tp}$	$V_{dsp} < V_{gsp} - V_{tp}$
	$V_{out} > V_{in} - V_{tp}$	**$V_{out} < V_{in} - V_{tp}$**

$$V_{gsp} = V_{in} - V_{DD}$$

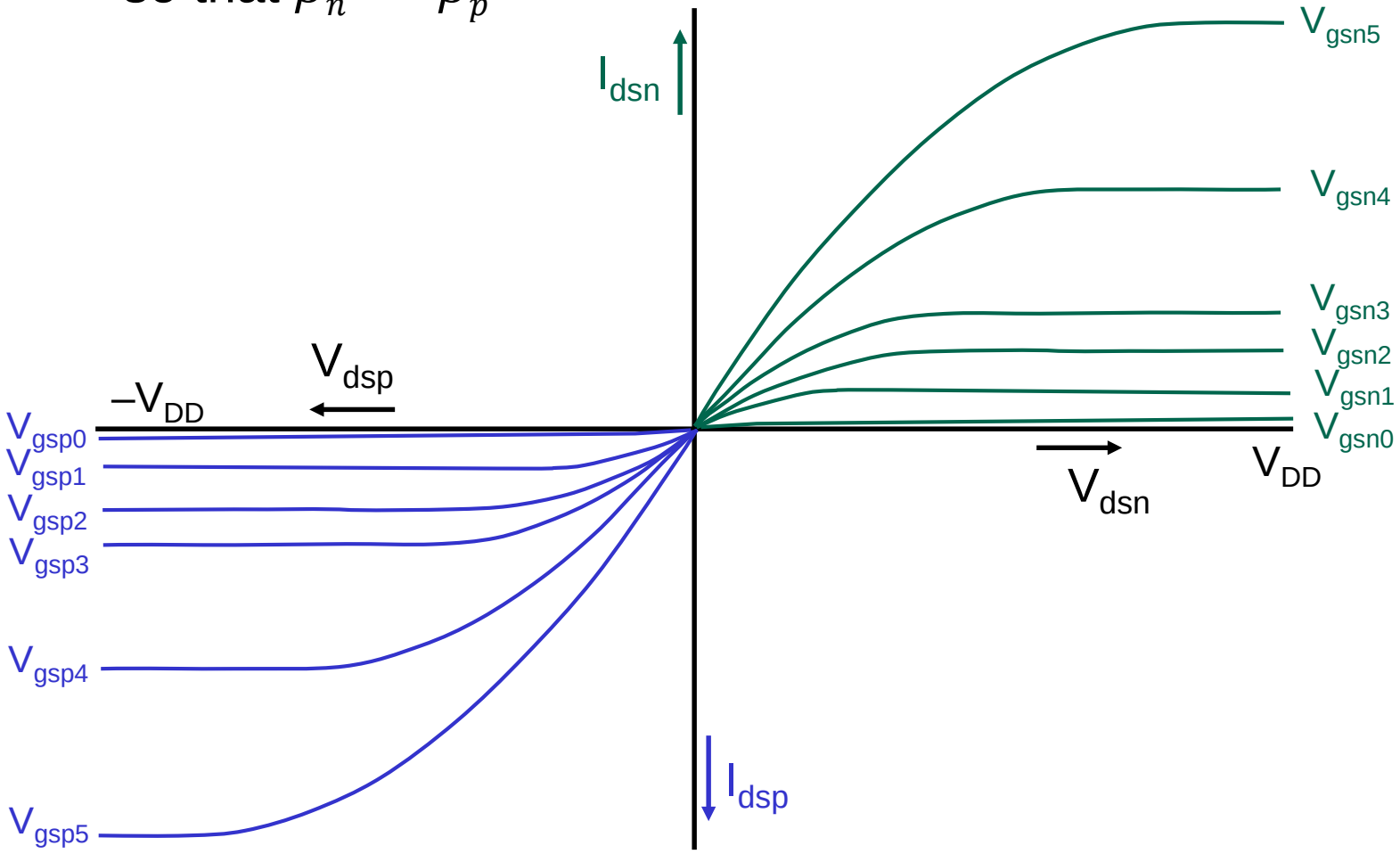
$$V_{dsp} = V_{out} - V_{DD}$$

(remember: V_{dsp} and $V_{tp} < 0$)

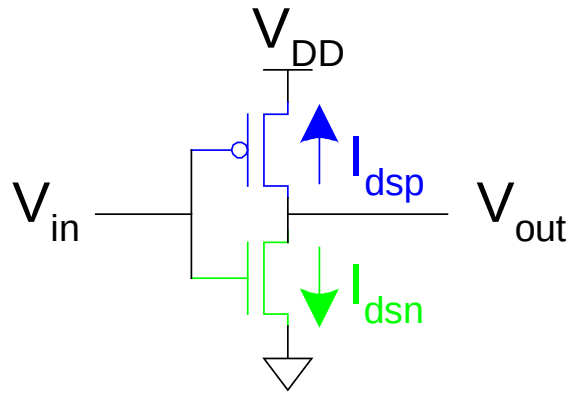


I-V Characteristics

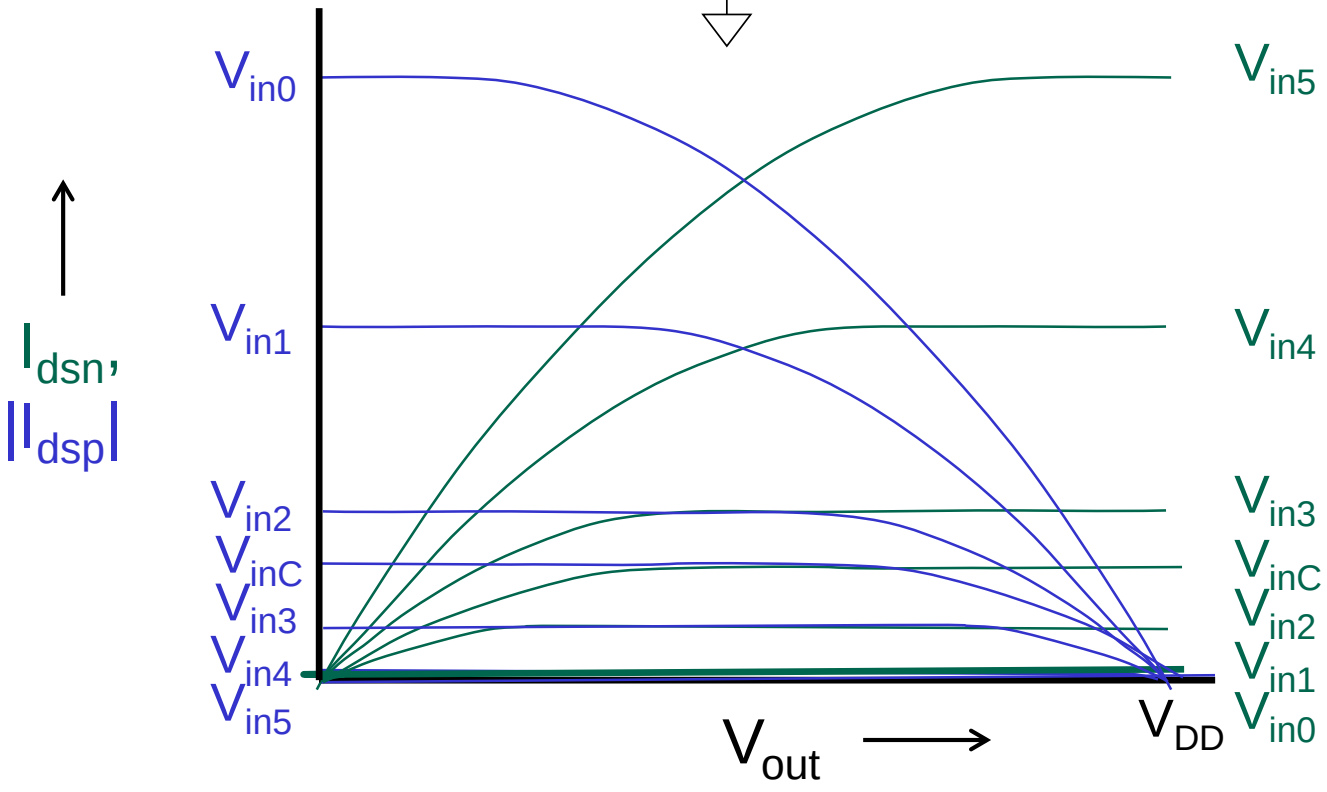
- Mobility of holes is 2-3x less than mobility of electrons
- Usually make pMOS 2x wider than nMOS
  - so that $\beta_n \approx \beta_p$



Replot I-V as function of V_{out} & V_{in}

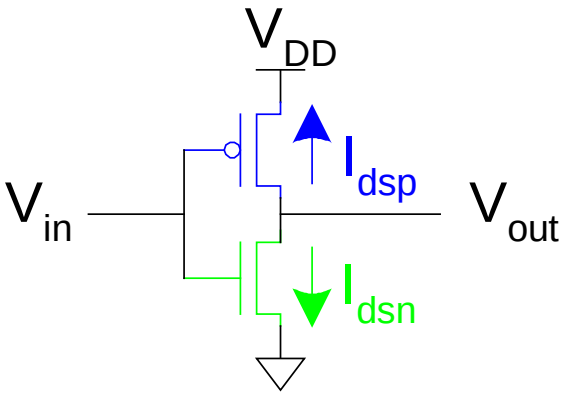


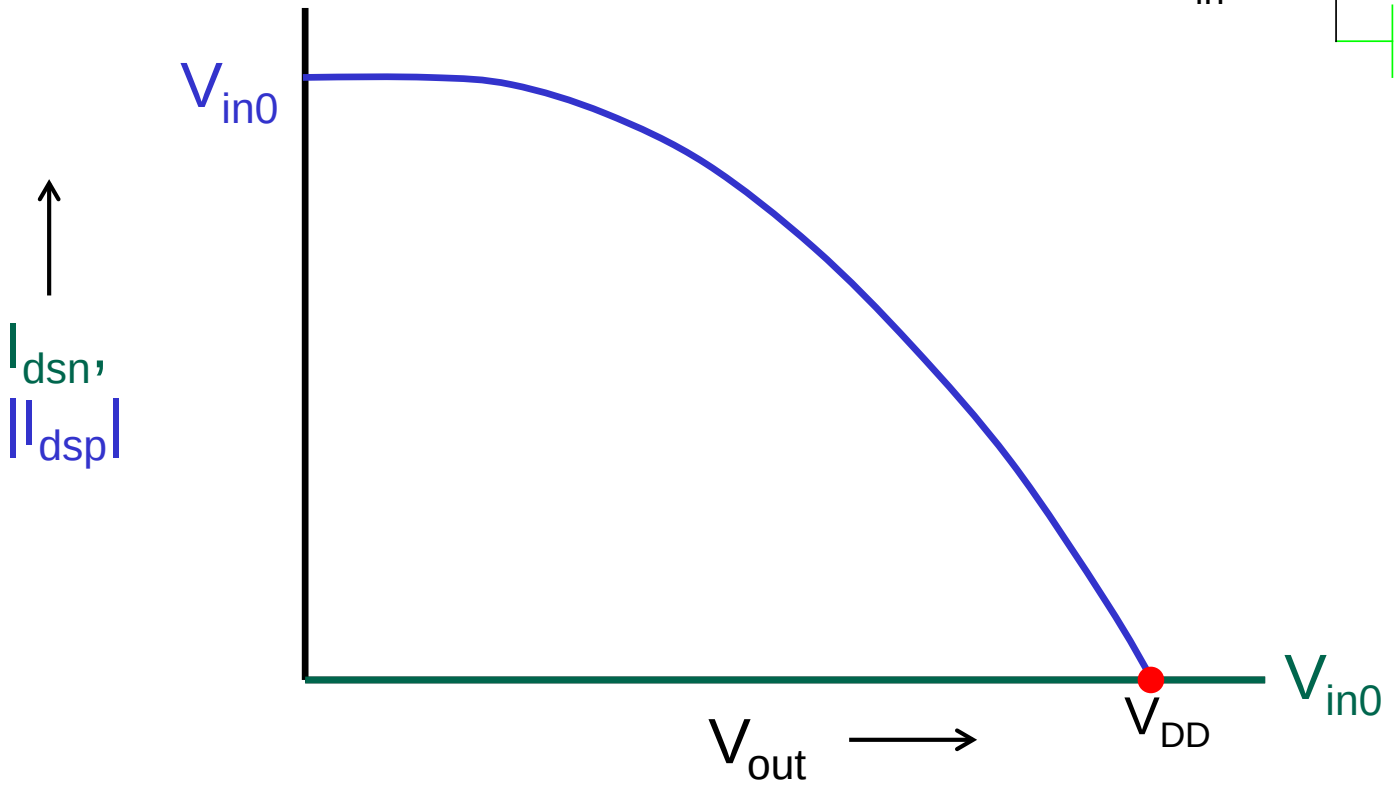
V_{out} is where $I_{dn} = -I_{dp}$



Load Line Analysis

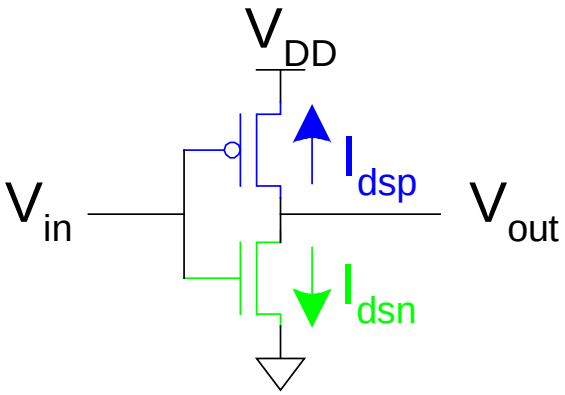
- $V_{in} = 0$

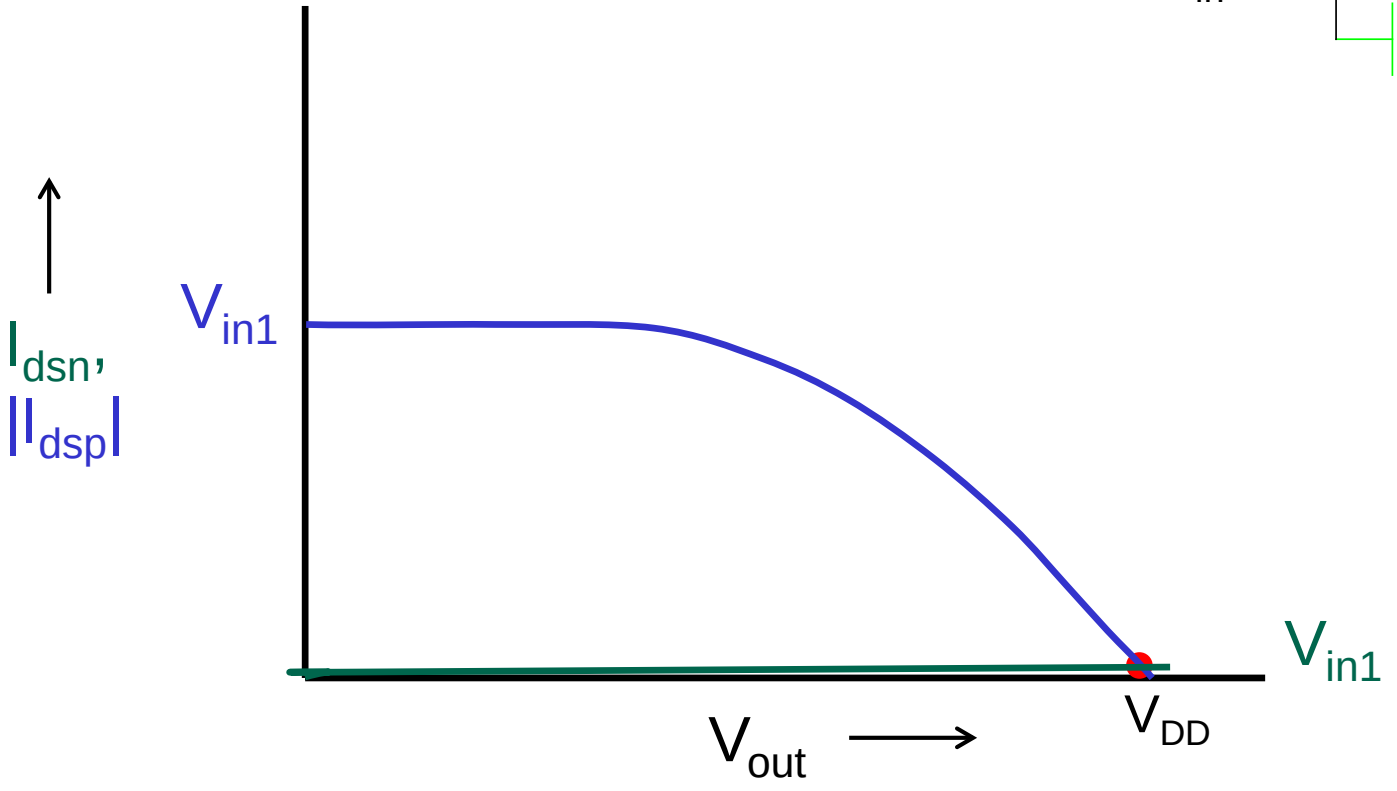




Load Line Analysis

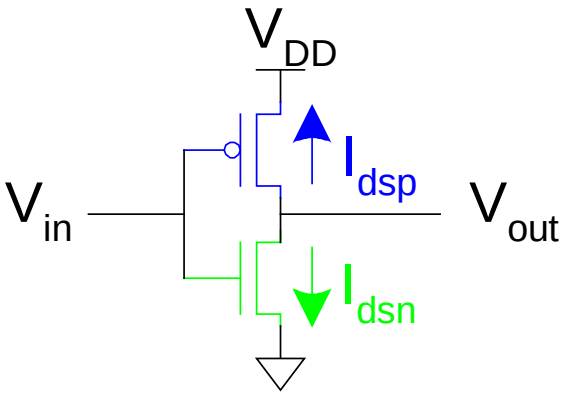
- $V_{in} = 0.2V_{DD}$

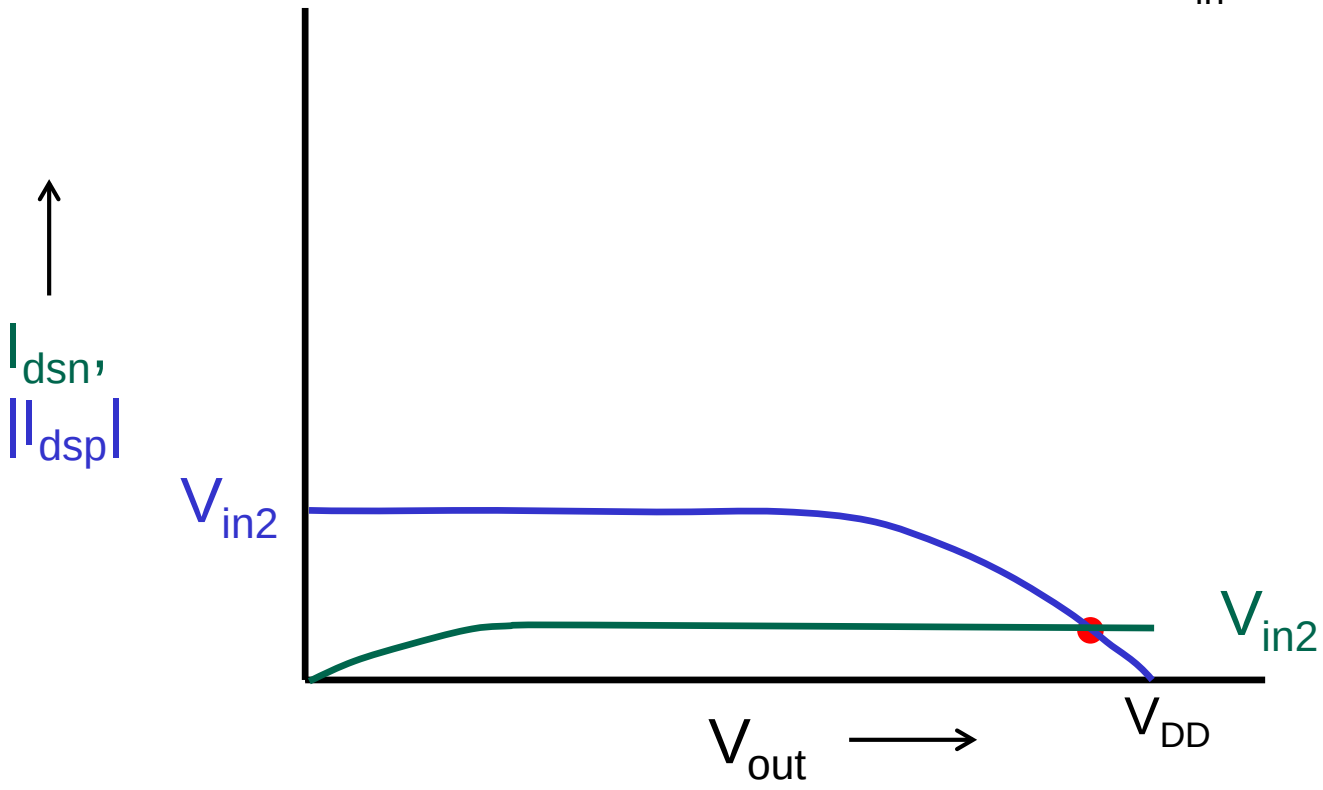




Load Line Analysis

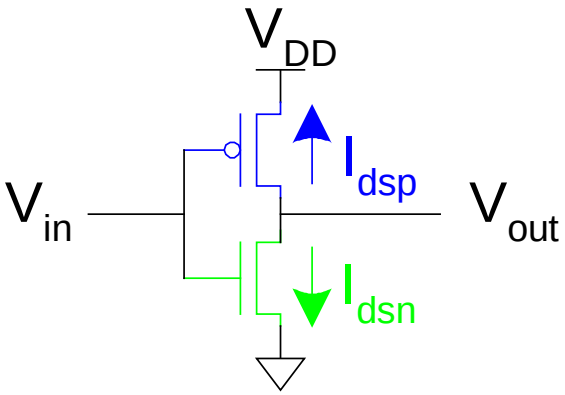
- $V_{in} = 0.4V_{DD}$

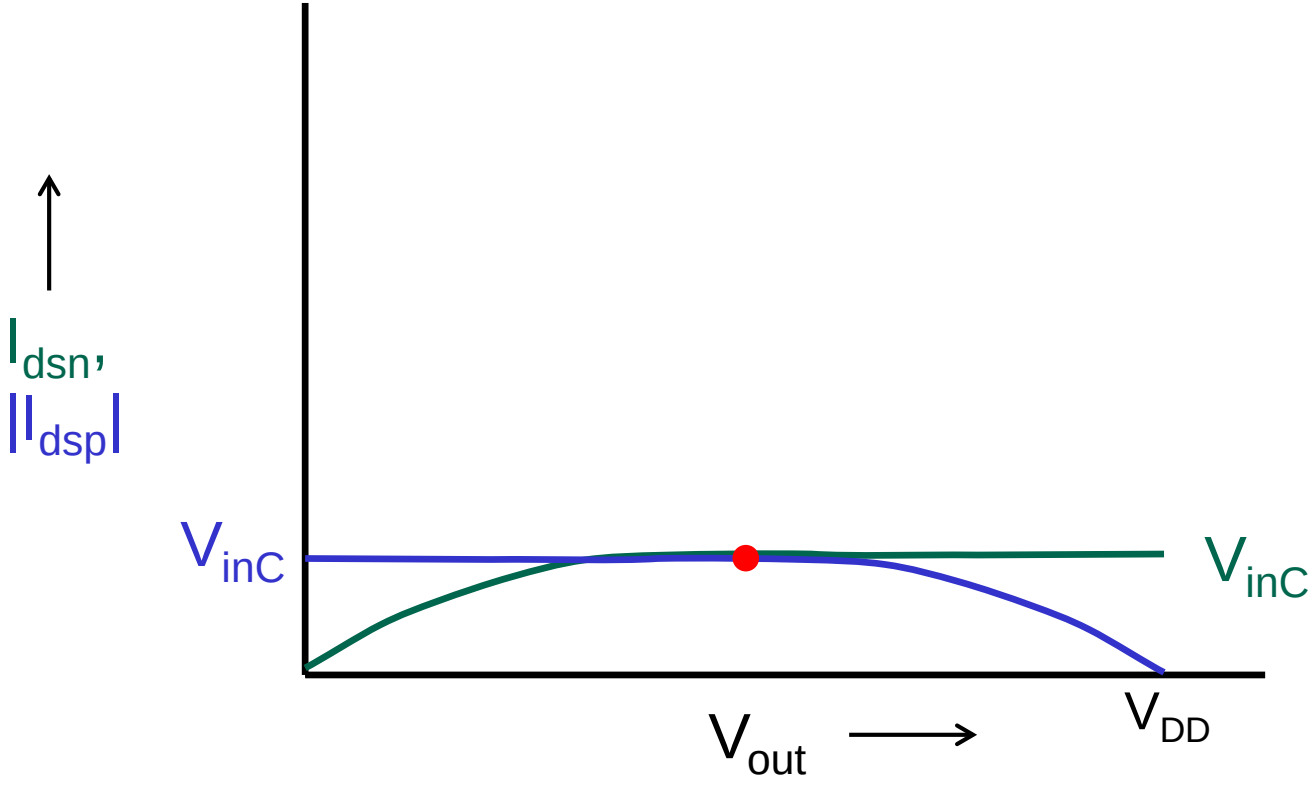




Load Line Analysis

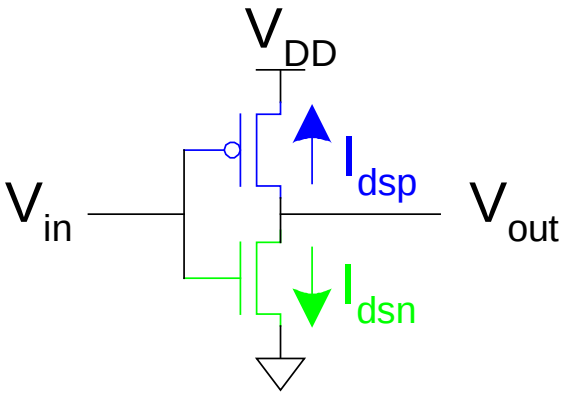
- $V_{in} = 0.5V_{DD}$

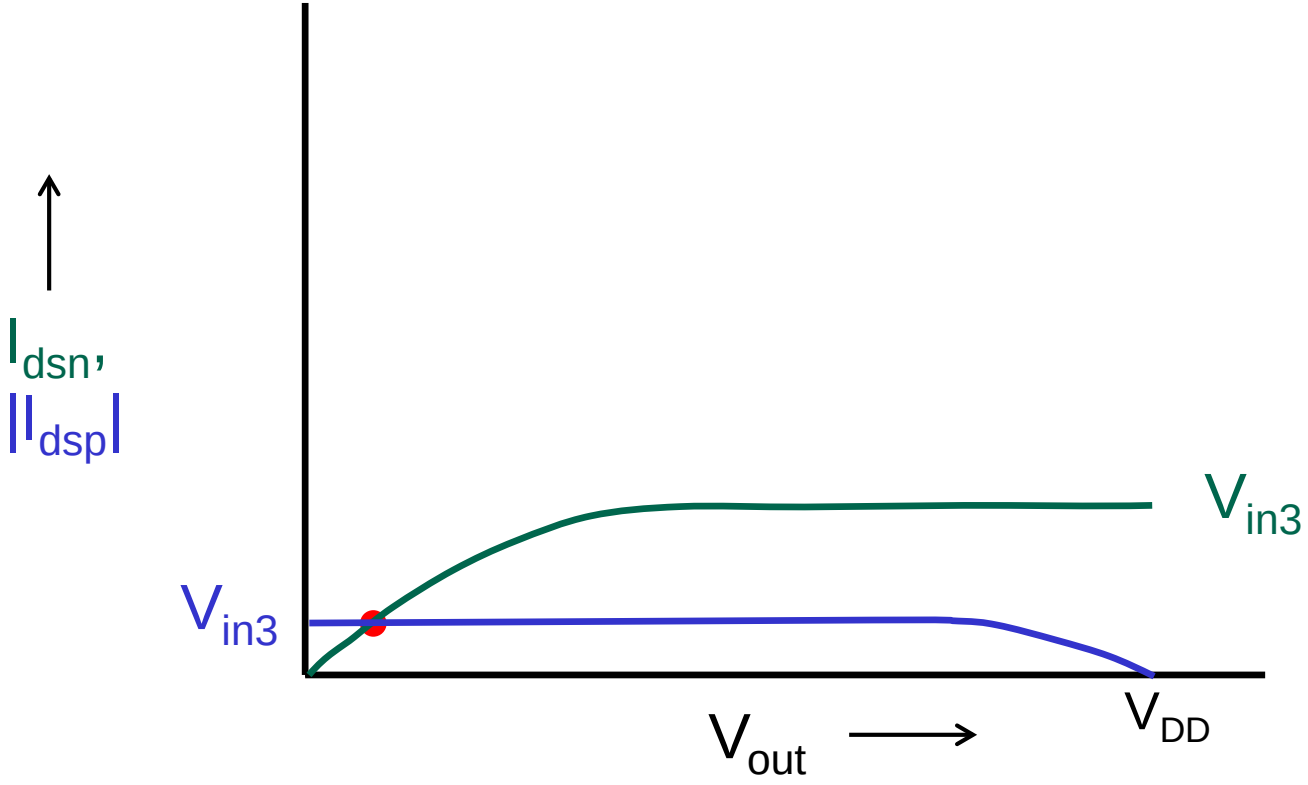




Load Line Analysis

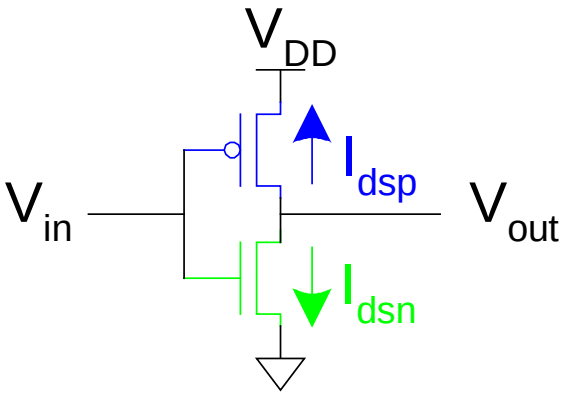
- $V_{in} = 0.6V_{DD}$

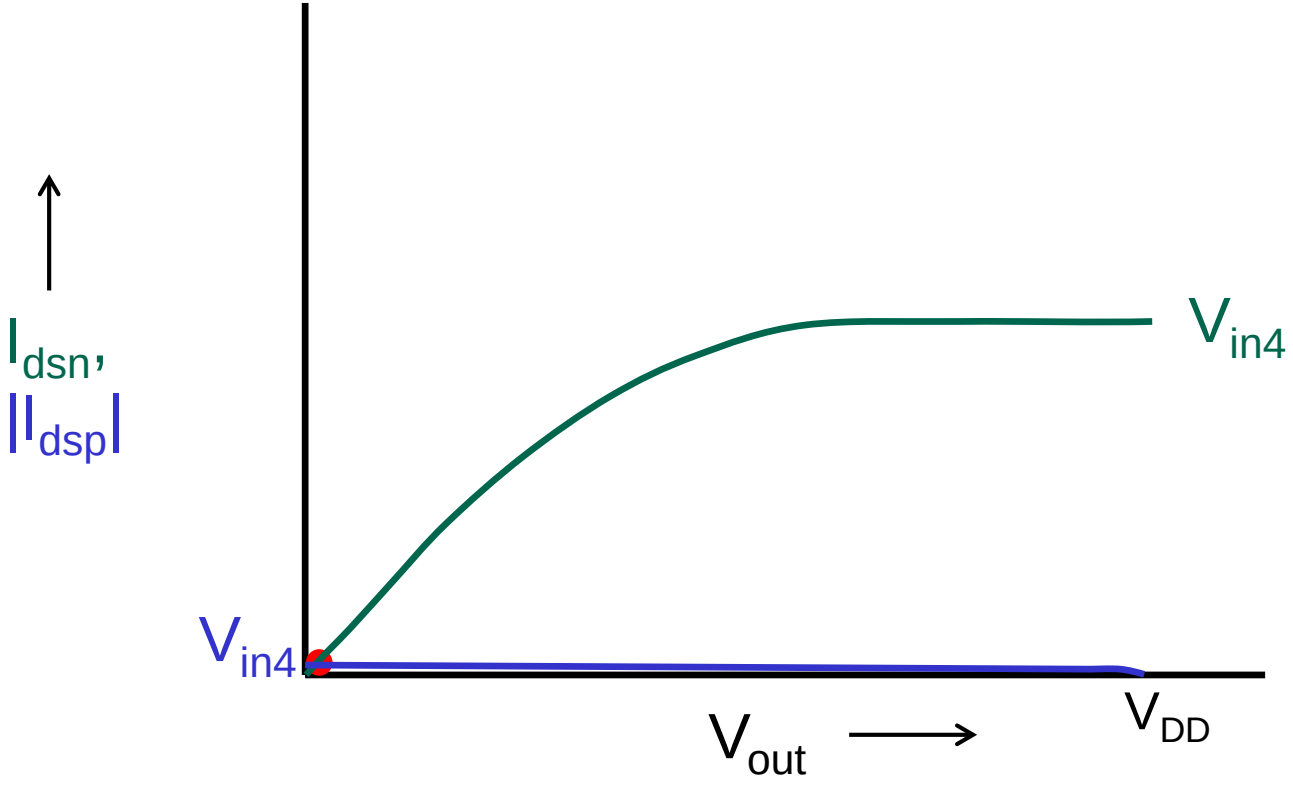




Load Line Analysis

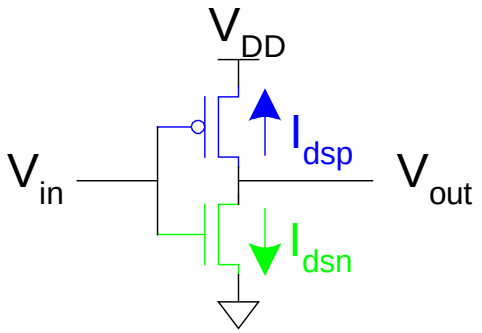
- $V_{in} = 0.8V_{DD}$

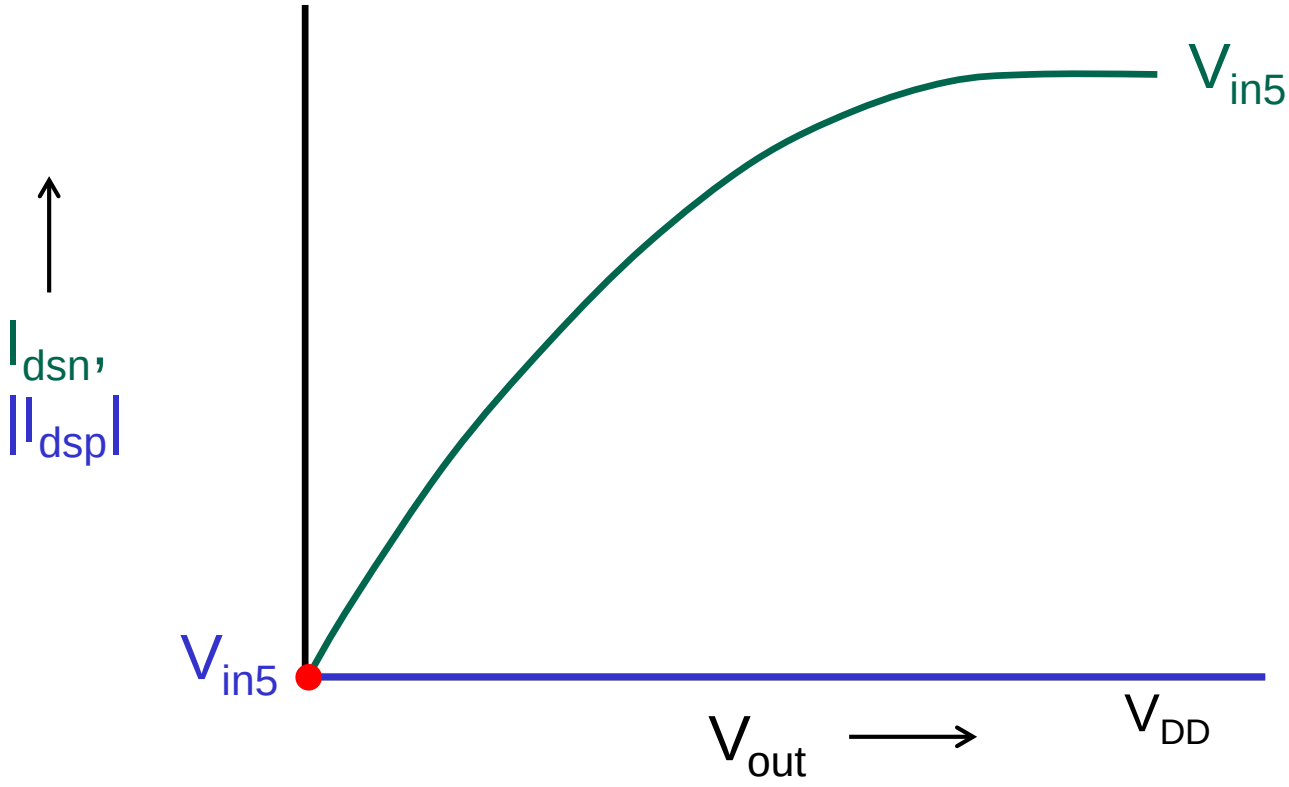




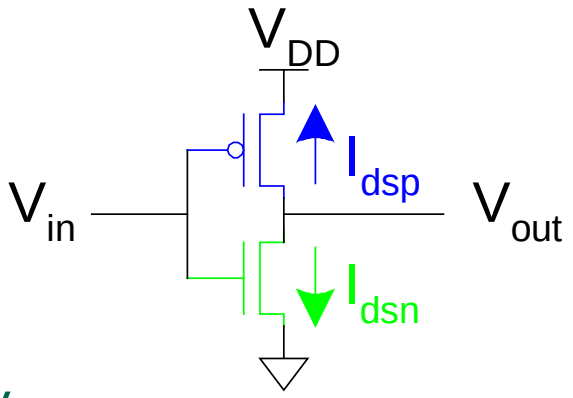
Load Line Analysis

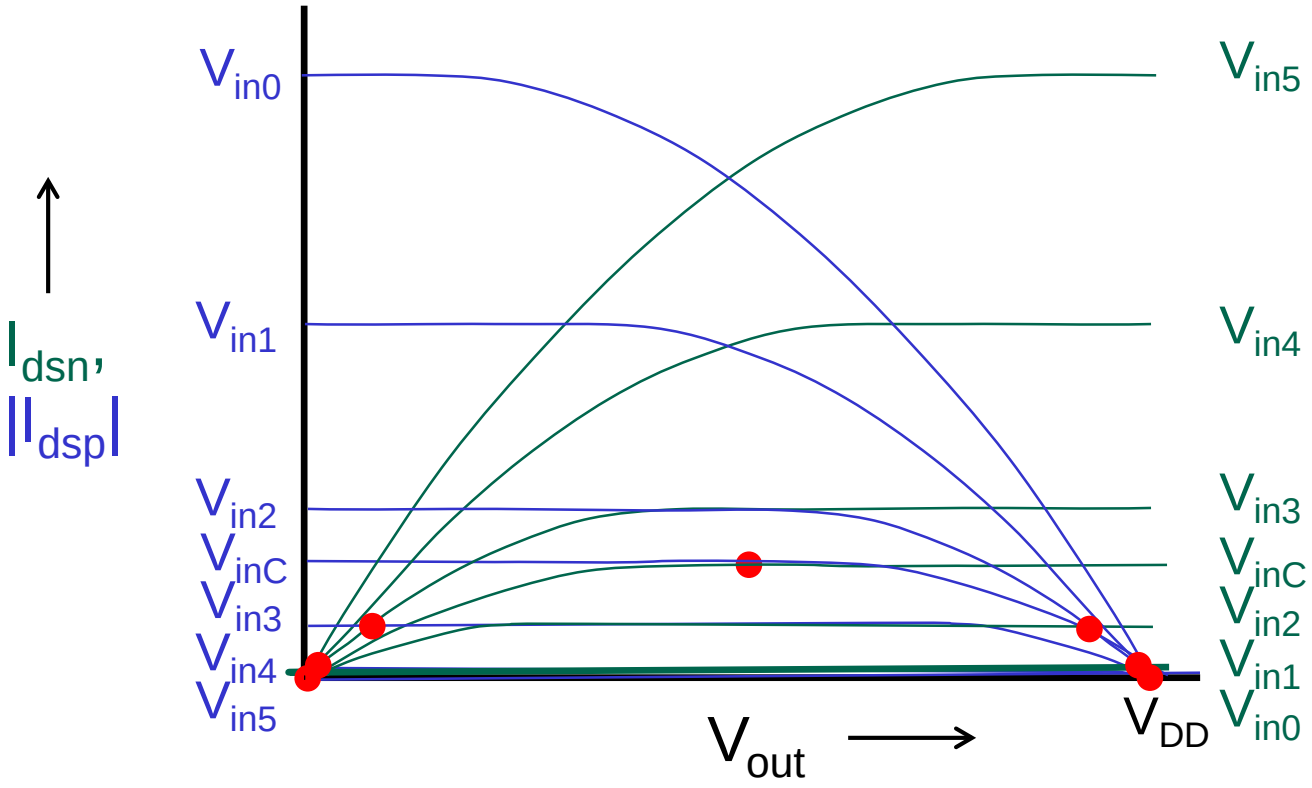
- $V_{in} = V_{DD}$





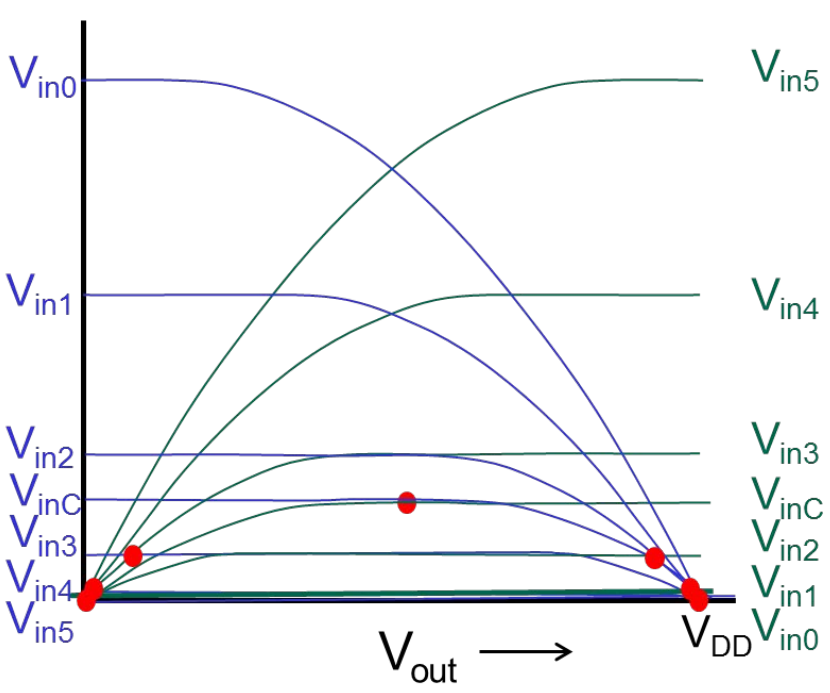
Load Line Analysis

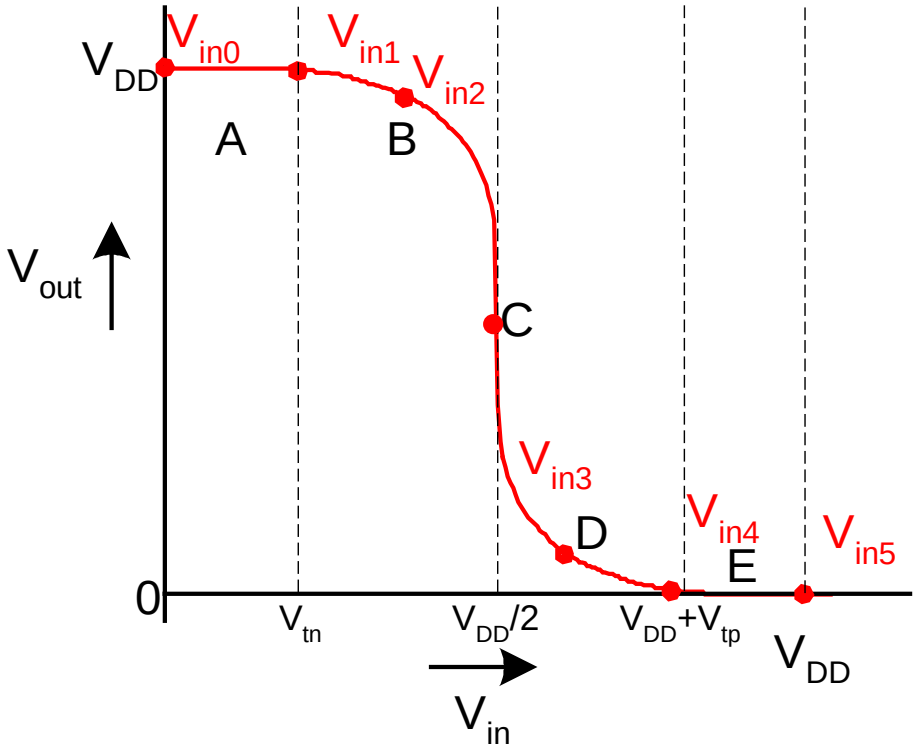




DC Transfer Curve

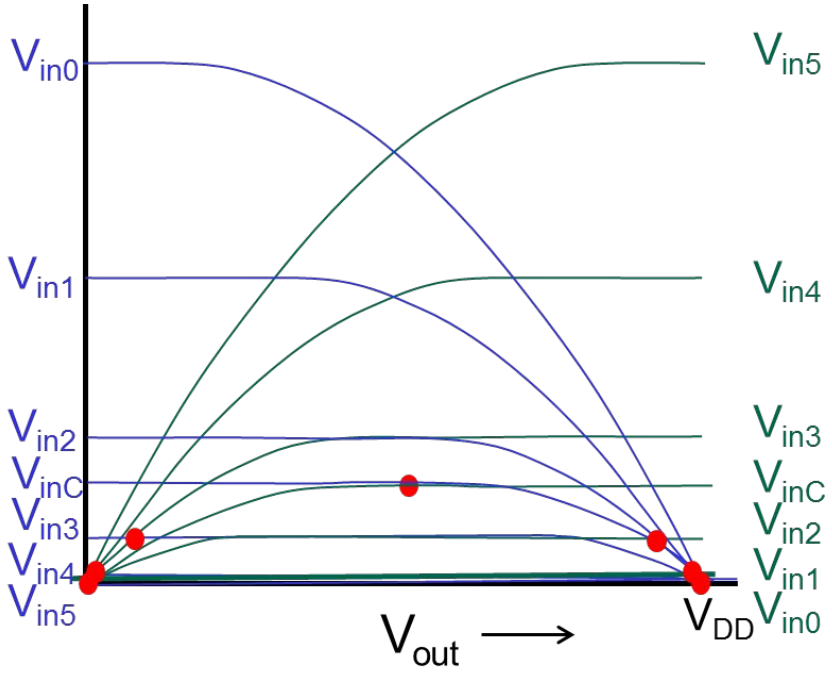
- Trans-scribe points onto V_{in} vs. V_{out} plot

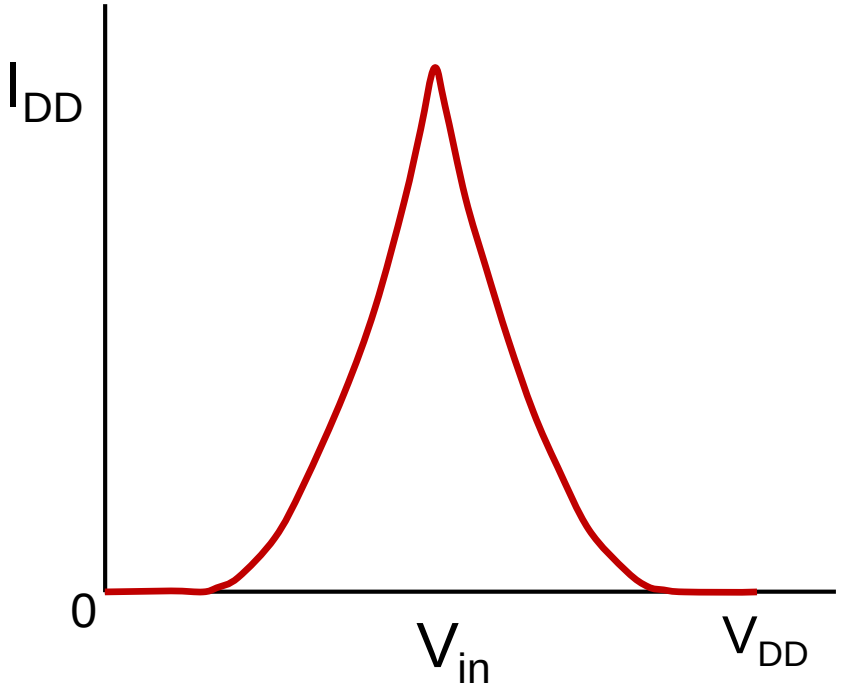




Supply Current

- $I_{DD} = I_{dsn} = -I_{dsp}$

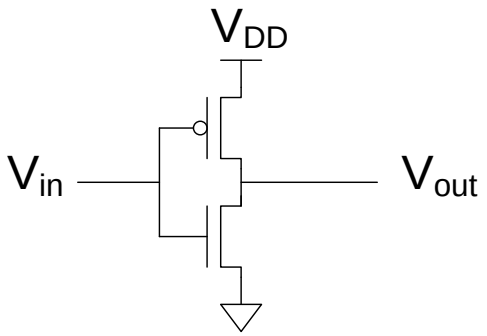




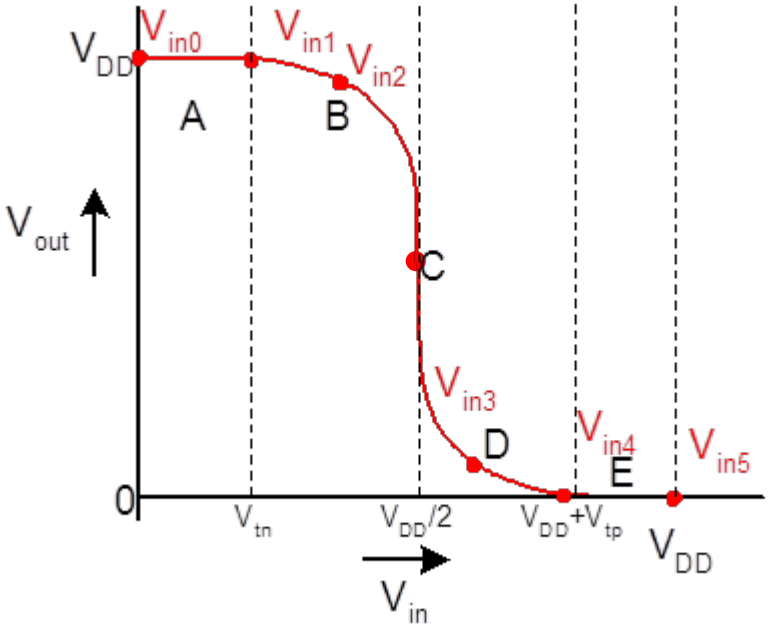
- Zero current when in normal logic range
- Transient current pulse drawn from V_{DD} supply on each switching event

Operating Regions

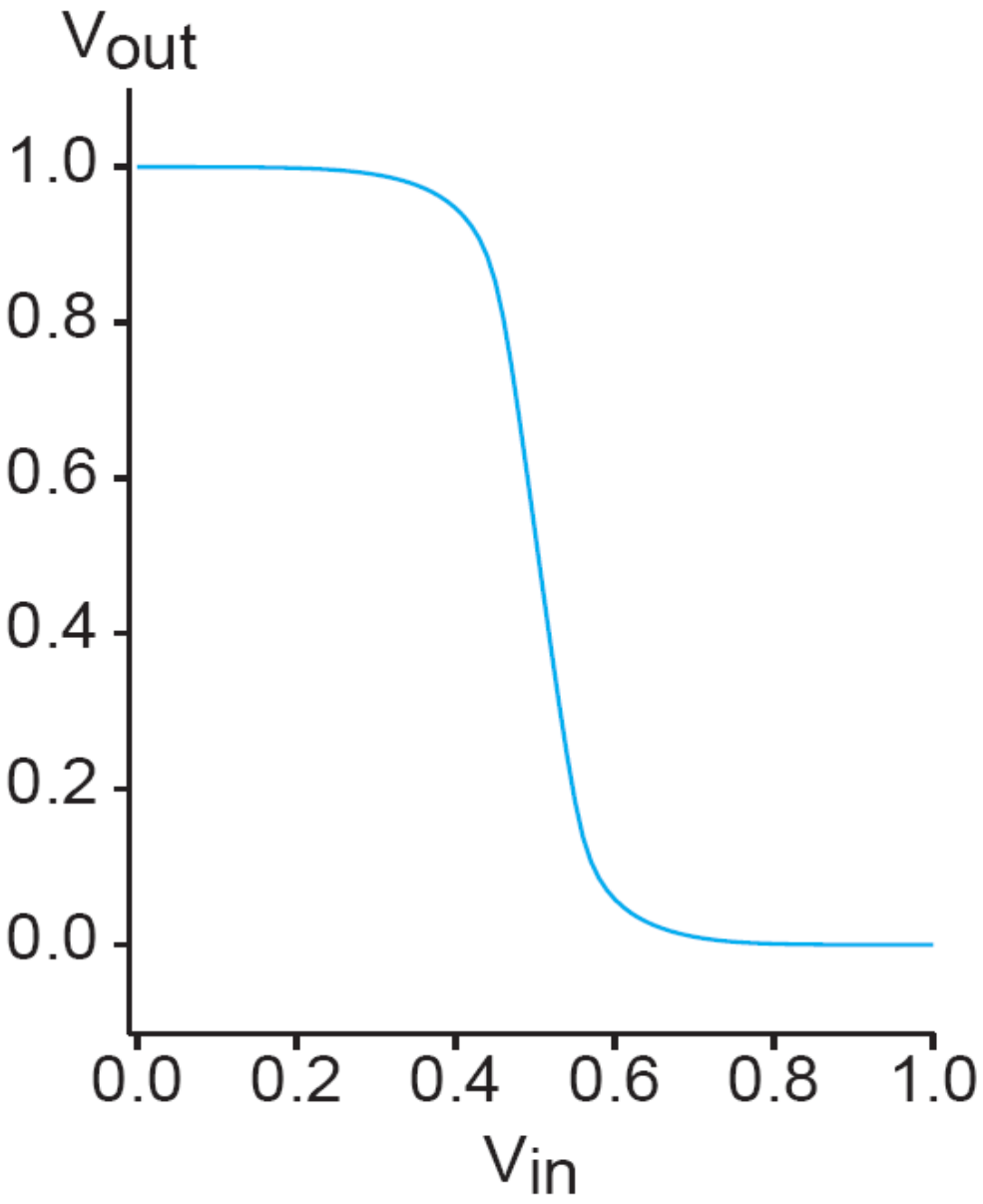
- Re-visit operating regions



Region	nMOS	pMOS
A	Cutoff	Linear
B	Saturation	Linear
C	Saturation	Saturation
D	Linear	Saturation
E	Linear	Cutoff

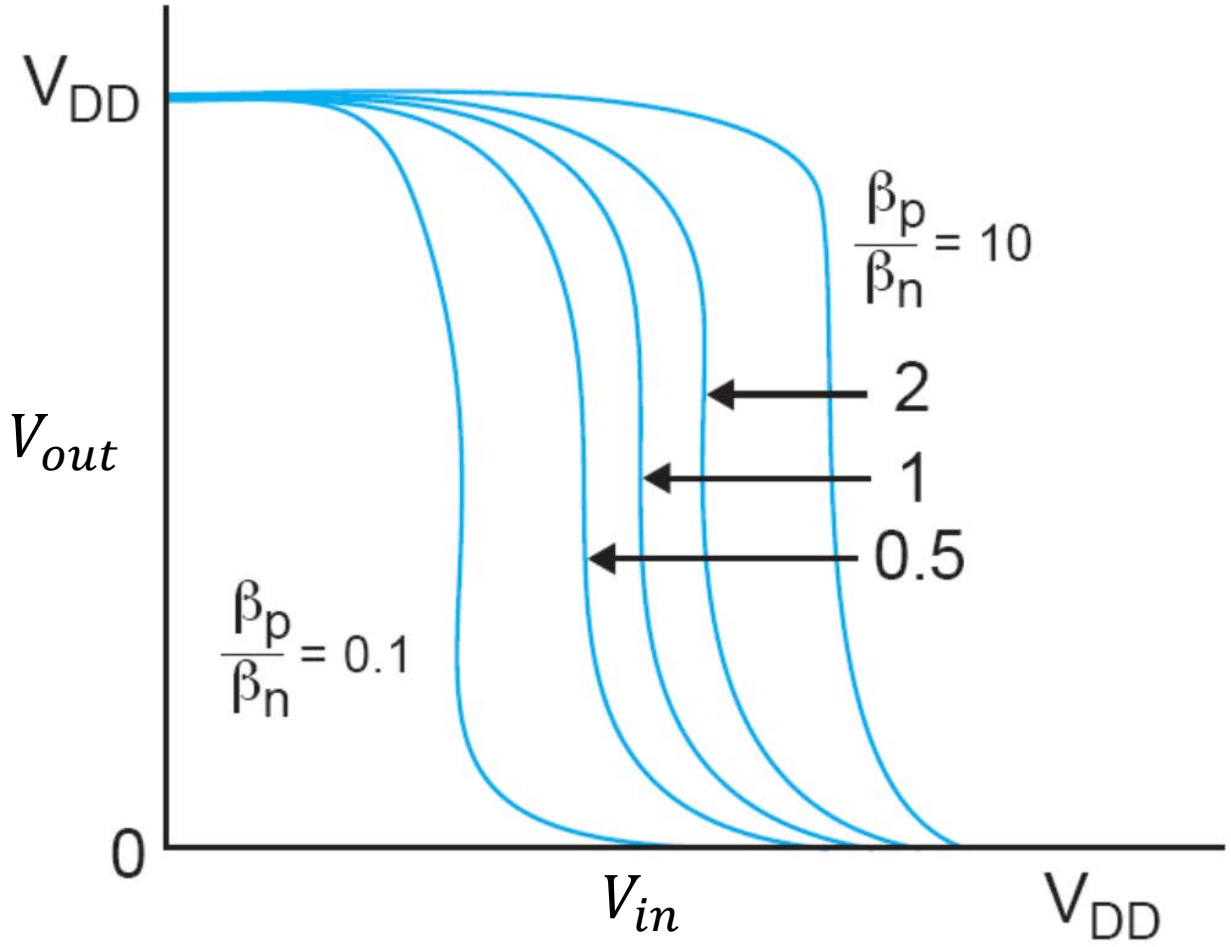


Simulated 65nm DC Characteristic



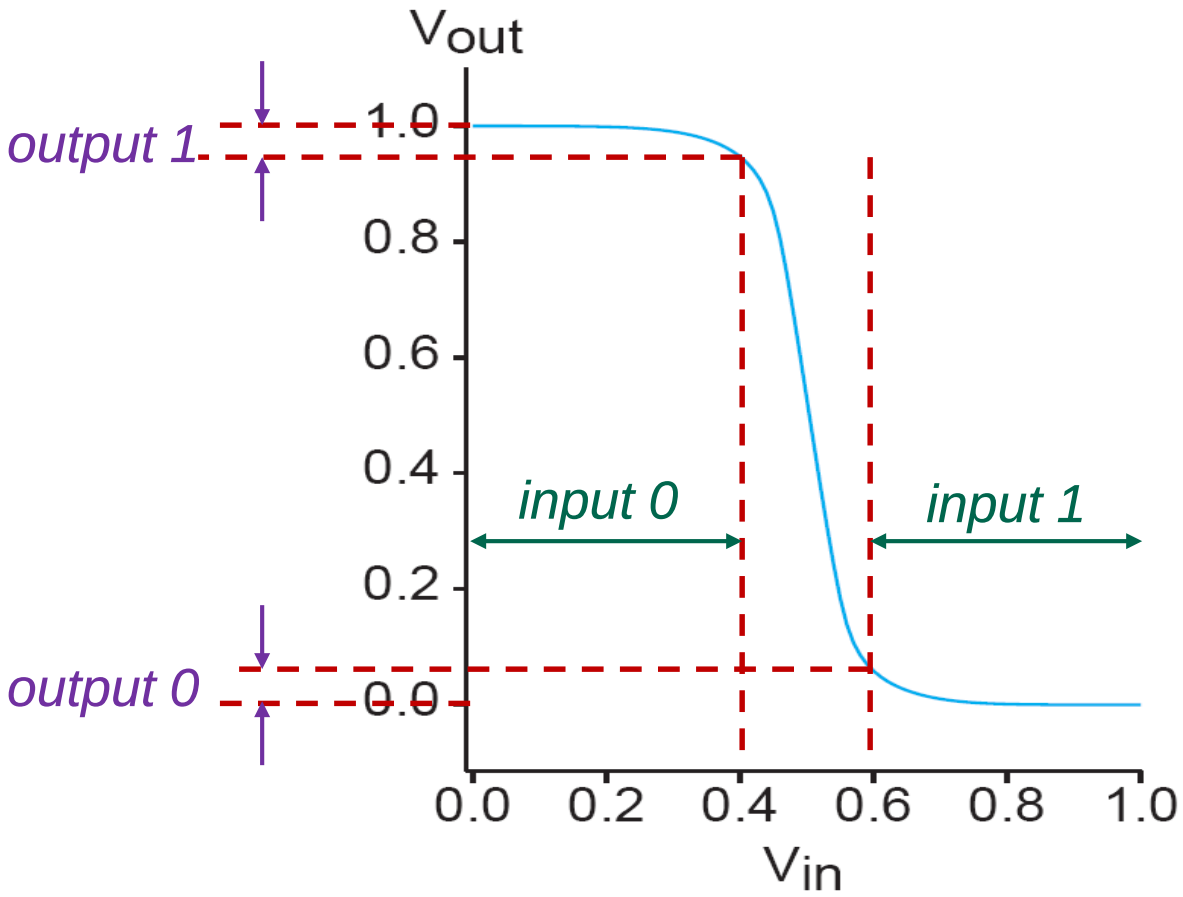
Beta Ratio

- If $\beta_p / \beta_n \neq 1$, switching point will move from $V_{DD}/2$
- Called *skewed* gate
- Other gates: collapse into equivalent inverter



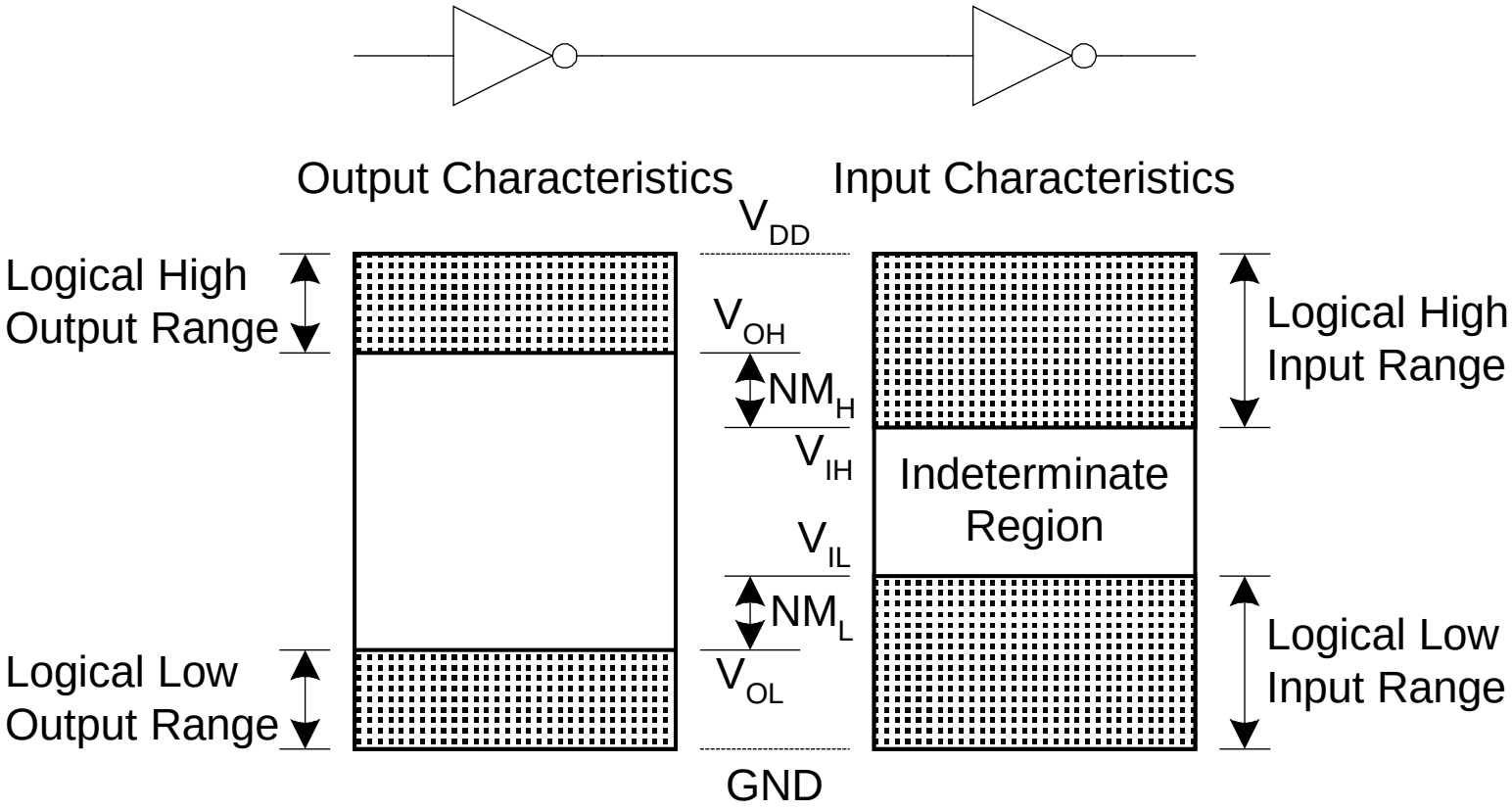
Restoring Logic

- Reason that we can build digital circuits with millions of gates and always get same answer is:
- Most CMOS logic gates are “restoring”
  - output logic level is better than input logic level



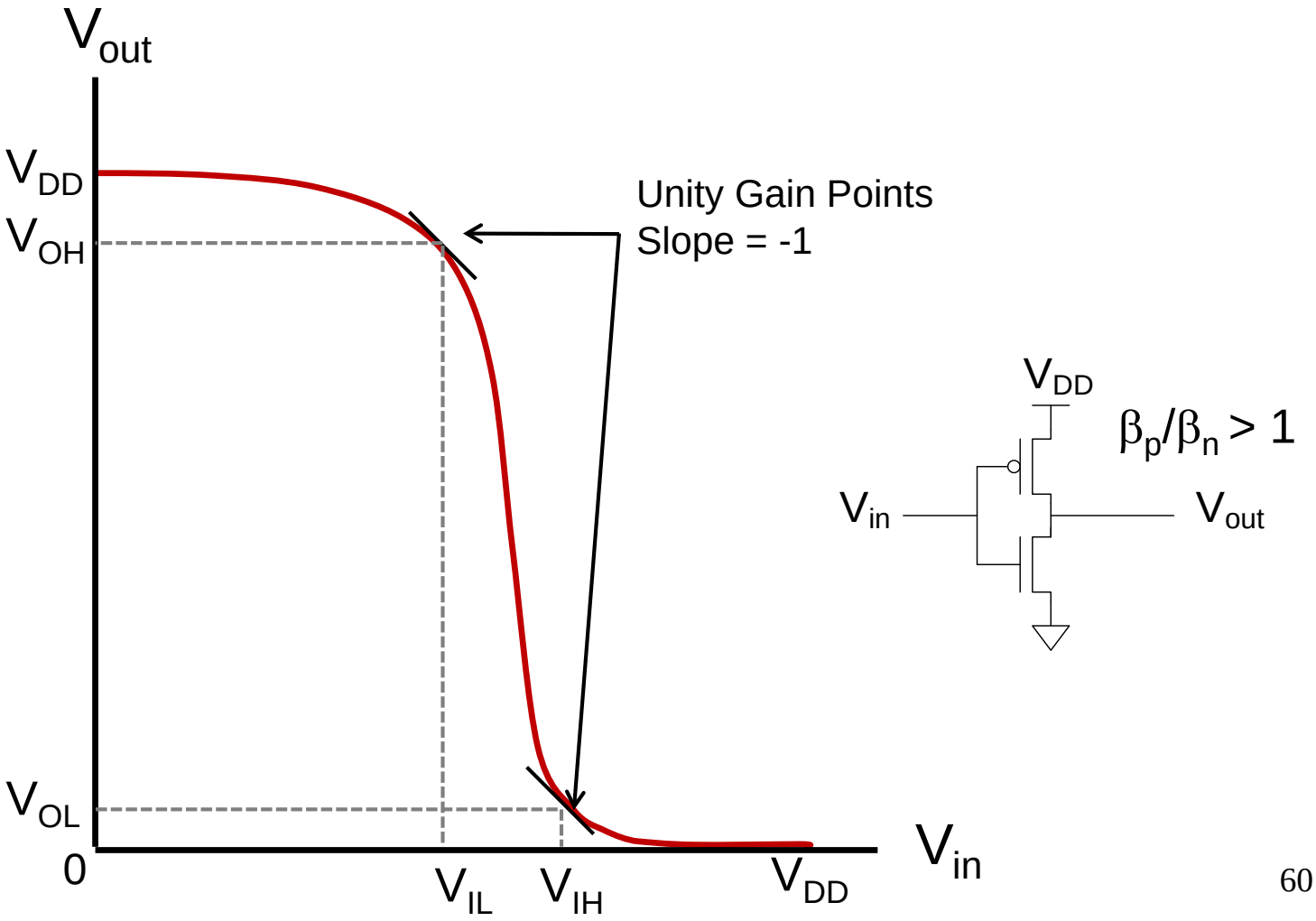
Noise Margins

- How much noise can a gate input see before it does not recognize the input?



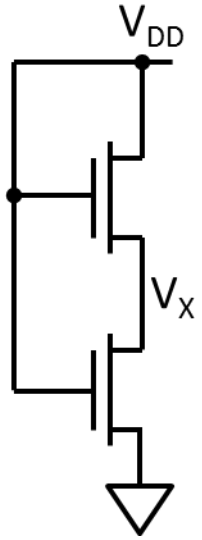
Nominal Logic Levels

- To maximize noise margins, select worst case logic levels at
  - unity gain point of DC transfer characteristic



Example: MOS IV Formula

Suppose we connect two identical nMOS devices in series between VDD and GND and connect the gates of each to VDD:



Assuming $V_{DD} > V_T$,

1. In which region is the upper transistor operating? Why?
2. In which region is the lower transistor operating? Why?
3. Derive an expression for the voltage V_x at the intermediate node (assume m=1).