Digital Systems Design – CPE 487

School of Engineering and Science

Spring 2018

Meeting Times:	Wednesday 12:00 – 12:50 pm Carnegie 316
	Friday 10:00 – 11:40 am Carnegie 316
Instructor:	Prof. Bryan Ackland
Contact Info:	Burchard 211, backland@stevens.edu, (201) 216-8096
Office Hours:	Wednesday 9:30 am – 11:30 am
	Thursday 10:00 am – 12:00 noon
	Other times by appt. or just stop by my office
Course Web:	http://personal.stevens.edu/~backland/Courses/Course487_Spring_18.htm
Prerequisite(s):	E 245 – Circuits and Systems
Corequisite(s):	None
Cross-listed with:	None

COURSE DESCRIPTION

The course focuses on digital system design, modeling and synthesis using the VHSIC (Very High Speed Integrated Circuits) Hardware Description Language (VHDL). The course begins with a review of Boolean logic and binary arithmetic. Students then learn modeling and simulation of digital circuits using behavioral, dataflow and structural modeling techniques, including the use of VHDL subprograms and operator overloading. This is followed by computer-aided synthesis and implementation, including finite state machines (FSM) and test bench design. Students will use commercial VHDL compilation, simulation and synthesis tools to evaluate and test their designs. They will also participate in several laboratory sessions in which they develop and test hardware implementations using commercial FPGA evaluation boards.

LEARNING OBJECTIVES

After successful completion of this course, students will be able to…

- Develop technical documentation of a complex digital system using hardware description language and schematic representations and to evaluate the correct function and performance based on simulations of the system.
- Apply VHDL entity/architecture modeling to represent component inputs and outputs and also internal signals, variables and operations.
- Develop VHDL models of systems using behavioral, structural and dataflow concepts to describe the internal behavior and/or structure of the design.
- Efficiently model a complex digital system as a hierarchy of interconnected components, taking advantage of regularity and component re-use.

- Build VHDL models of complex digital circuits suitable for synthesis where the target platform is an FPGA or ASIC logic library. The student will understand the limitations of VHDL as a synthesis language and know which particular styles of VHDL coding lead to efficient solutions.
- Use VHDL to design complex synthesizable state machines using Mealy and/or Moore architectures.
- Write test vectors for a digital system and develop a VHDL test-bench to apply these vectors using file based input/output operations.
- Represent and document designs, perform simulations and synthesize implementations using software tools provided by an FPGA vendor.

FORMAT AND STRUCTURE

This course is comprised of two lectures (one 50 minute and one 100 minute) per week. There is also a laboratory component which is built into the lecture schedule. In the lab, students work in groups of three. Lab grades are incorporated into the final grade of this course.

COURSE MATERIALS

Textbook(s): VHDL - A Starter's Guide, Second Edition, Sudhakar Yalamanchili, Publisher: Prentice Hall, ISBN: 0-13-145735-7, 2005

Other Ref: (1) A VHDL Primer, 3rd edition, J. Bhasker, Prentice Hall, ISBN 0-13-096575-8, 1999

(2) Circuit Design with VHDL, V. A. Pedroni, MIT Press, ISBN: 0-262-16224-5, 2004.

Materials: None

COURSE REQUIREMENTS

Attendance Counts towards 5% of final grade. Each student is permitted (2) unexcused absences per semester without penalty.

Participation Up to (2) grade points bonus will be awarded to students who participate by frequently asking and answering questions in class

Homework There are usually six (6) homework assignments throughout the course as well as a design project. All assignments count equally towards 20% of the final grade except for the project which counts as three (3) homeworks. All assignments should be submitted on the due date during class to the professor via hard copy. Homework assignments will be graded and returned within two class periods.

Labs Lab grades are determined taking into account attendance, quality of participation and quality of report and count toward 20% of the final grade.

Exams There will be two exams in this course; a midterm and a final. The final exam is cumulative. The midterm will be taken in class according to the published class schedule. The final exam will normally take place during exam week; the time and place will be determined by the Registrar.

GRADING PROCEDURES

Grades will be based on:

Attendance	(5 %)
Homework	(20 %)

Lab	(20 %)
Midterm	(25 %)
Final	(30 %)

ACADEMIC INTEGRITY

Undergraduate Honor System

Enrollment into the undergraduate class of Stevens Institute of Technology signifies a student's commitment to the Honor System. Accordingly, the provisions of the Stevens Honor System apply to all undergraduate students in coursework and Honor Board proceedings. It is the responsibility of each student to become acquainted with and to uphold the ideals set forth in the Honor System Constitution. More information about the Honor System including the constitution, bylaws, investigative procedures, and the penalty matrix can be found online at http://web.stevens.edu/honor/

The following pledge shall be written in full and signed by every student on all submitted work (including, but not limited to, homework, projects, lab reports, code, quizzes and exams) that is assigned by the course instructor. No work shall be graded unless the pledge is written in full and signed.

"*I pledge my honor that I have abided by the Stevens Honor System*."

Reporting Honor System Violations

Students who believe a violation of the Honor System has been committed should report it within ten business days of the suspected violation. Students have the option to remain anonymous and can report violations online at www.stevens.edu/honor.

EXAM ROOM CONDITIONS

The following procedures apply to exams for this course. As the instructor, I reserve the right to modify any conditions set forth below by printing revised Exam Room Conditions on the exam.

1. Students may use the following devices during exams. Any electronic devices that are not mentioned in the list below are not permitted.

Device	**Permitted?**	
	Yes	No
Laptops		X
Cell Phones		X
Tablets		X
Smart Watches		X
Google Glass		X
Stand-alone calculator	X	

2. Students may use the following materials during exams. Any materials that are not mentioned in the list below are not permitted.

Material	**Permitted?**	
	Yes	No
Handwritten Notes	X	
Typed Notes	X	
Textbooks	X	

Other reference books	X	

3. Students are not allowed to work with or talk to other students during exams.

LEARNING ACCOMODATIONS

Stevens Institute of Technology is dedicated to providing appropriate accommodations to students with documented disabilities. Student Counseling and Disability Services works with undergraduate and graduate students with learning disabilities, attention deficit-hyperactivity disorders, physical disabilities, sensory impairments, and psychiatric disorders in order to help students achieve their academic and personal potential. They facilitate equal access to the educational programs and opportunities offered at Stevens and coordinate reasonable accommodations for eligible students. These services are designed to encourage independence and self-advocacy with support from SCDS staff. The SCDS staff will facilitate the provision of accommodations on a case-by-case basis. These academic accommodations are provided at no cost to the student.

Disability Services Confidentiality Policy

Student Disability Files are kept separate from academic files and are stored in a secure location within the office of Student Counseling, Psychological & Disability Services. The Family Educational Rights Privacy Act (FERPA, 20 U.S.C. 1232g; 34CFR, Part 99) regulates disclosure of disability documentation and records maintained by Stevens Disability Services. According to this act, prior written consent by the student is required before our Disability Services office may release disability documentation or records to anyone. An exception is made in unusual circumstances, such as the case of health and safety emergencies.

For more information about Disability Services and the process to receive accommodations, visit https://www.stevens.edu/sit/counseling/disability-services. If you have any questions please contact:

Lauren Poleyeff, Psy.M., LCSW - Disability Services Coordinator and Staff Clinician in Student Counseling and Disability Services at Stevens Institute of Technology at lpoleyef@stevens.edu or by phone (201) 216-8728.

INCLUSIVITY STATEMENT

Stevens Institute of Technology believes that diversity and inclusiveness are essential to excellence in education and innovation. Our community represents a rich variety of backgrounds, experiences, demographics and perspectives and Stevens is committed to fostering a learning environment where every individual is respected and engaged. To facilitate a dynamic and inclusive educational experience, we ask all members of the community to:

- be open to the perspectives of others
- appreciate the uniqueness their colleagues
- take advantage of the opportunity to learn from each other
- exchange experiences, values and beliefs
- communicate in a respectful manner
- be aware of individuals who are marginalized and involve them
- keep confidential discussions private

TYPICAL COURSE SCHEDULE

(Summer schedule is accelerated – completes in 7 weeks)
(Go to course website for exact schedule and homework due dates)

Week	Topic(s)	Notes	Homeworks
1	Class organization Overview of Digital System Design	Lecture 0 Lecture 1	HW1
	Boolean Logic & Binary Arithmetic Introduction to VHDL	Lecture 2 Lecture 3	
2	Entities, Architectures & Signals	Lecture 4	HW2
	Dataflow Modeling	Lecture 5	
3	Behavioral Modeling (I)	Lecture 6	
			HW3
4	Using Xilinx Toolsets		
	Behavioral Modeling (II)	Lecture 7	HW4
5	Structural Modeling	Lecture 8	HW3
	Generics & Configurations	Lecture 9	
6	Midterm Review		
	Midterm Exam		
7	Midterm Solutions		Project
	Lab 1		
8	Subprograms & Overloading	Lecture 10	
	Lab 2		
9	Packages & Libraries	Lecture 11	HW5
	Lab 3		
10	VHDL for Synthesis (I)	Lecture 12	
	Lab 4		
11	VHDL for Synthesis (II)		HW6

	Lab 5		
12	Finite State Machines (I)	Lecture 13	
	Lab 6		
13	Finite State Machines (II)		
			HW7
14	Test Bench	Lecture 14	
	Final Review		
15	Final Exam		