CPE 487: Digital System Design

HW5

Due: 4/11/2018

1: Functions (10 points)

Create a function *transitions* that takes as input a value of type std_logic of arbitrary length. The returned value should be an integer that records the number of transitions (0 → 1, or 1 → 0) as you scan the binary bit pattern from left to right (or right to left). For example, the value 0110010011 would return 5; the value 001 would return 1.

Below is a piece of VHDL code that you can use to test your function. Add your function to the code and simulate to check that your code is giving the correct result. Show your code and the simulation results. In your simulation, display the first 100 ns, with t2, t4, t6 and t8 all shown as either signed or unsigned decimal and data displayed as binary.

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

entity test_transitions is
end test_transitions;

architecture Behavioral of test_transitions is

signal data: std_logic_vector (7 downto 0):="01111100";
signal t8, t6, t4, t2: integer;

begin
tt:     process
        begin
                wait for 10 ns;
                data <= data+1;
        end process tt;

        t8 <= transitions(data);
        t6 <= transitions(data(5 downto 0));
        t4 <= transitions(data(3 downto 0));
        t2 <= transitions(data(1 downto 0));

end Behavioral;
```

2: Procedures (10 points)

Write a procedure that has five formal parameters A, B, C, MAX and SUM, all signals and all of type integer. When called, it sets MAX to the value (maximum of A, B and C) after 10ns and SUM to the value (A+B+C) after 15ns.

Write a program to test your procedure for a few different values of A, B and C

Show code and simulation results