CPE 487 Mid-Term Exam

- Friday March 9 @ 10:00 am in:
  - Carnegie 315 (last name A-K)
  - Carnegie 316 (last name L-Z)
- You can use lecture notes, homeworks and Yalamanchili text book
- No cell phones or on-line access

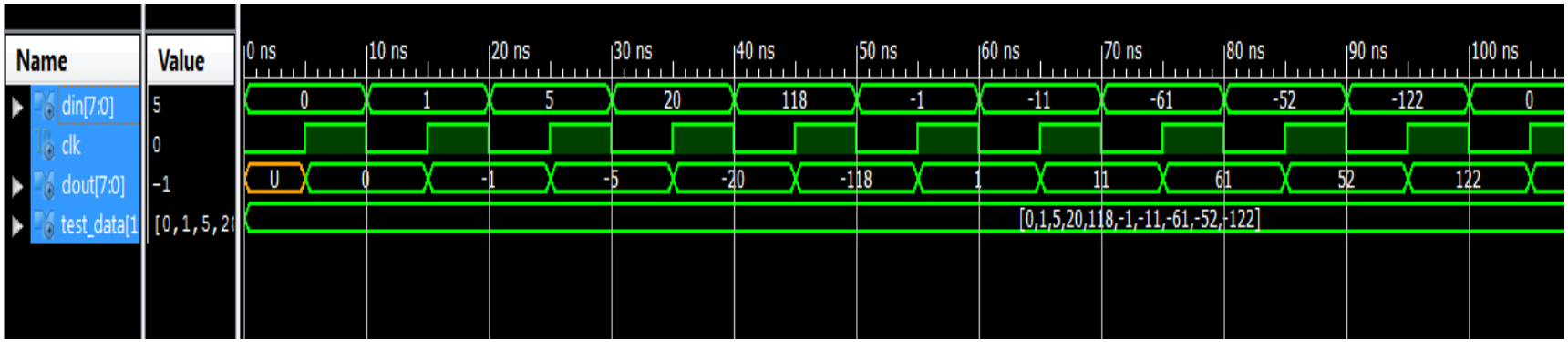
HW4 Solutions 1(a)

```
entity twos_comp is
    Port ( din : in  STD_LOGIC_VECTOR (7 downto 0);
           clk : in  STD_LOGIC;
           dout : out  STD_LOGIC_VECTOR (7 downto 0));
end twos_comp;

architecture Behavioral of twos_comp is

begin
   process(clk)
   variable one_test: integer;
   begin
      if clk = '1' then
         one_test := 0;
         for i in 0 to 7 loop
            if one_test > 0 then
               dout(i) <= not din(i);
            elsif din(i) = '1' then
               dout(i) <= '1';
               one_test := 1;
            else
               dout(i) <= '0';
            end if;
         end loop;
      end if;
   end process;

end Behavioral;
```

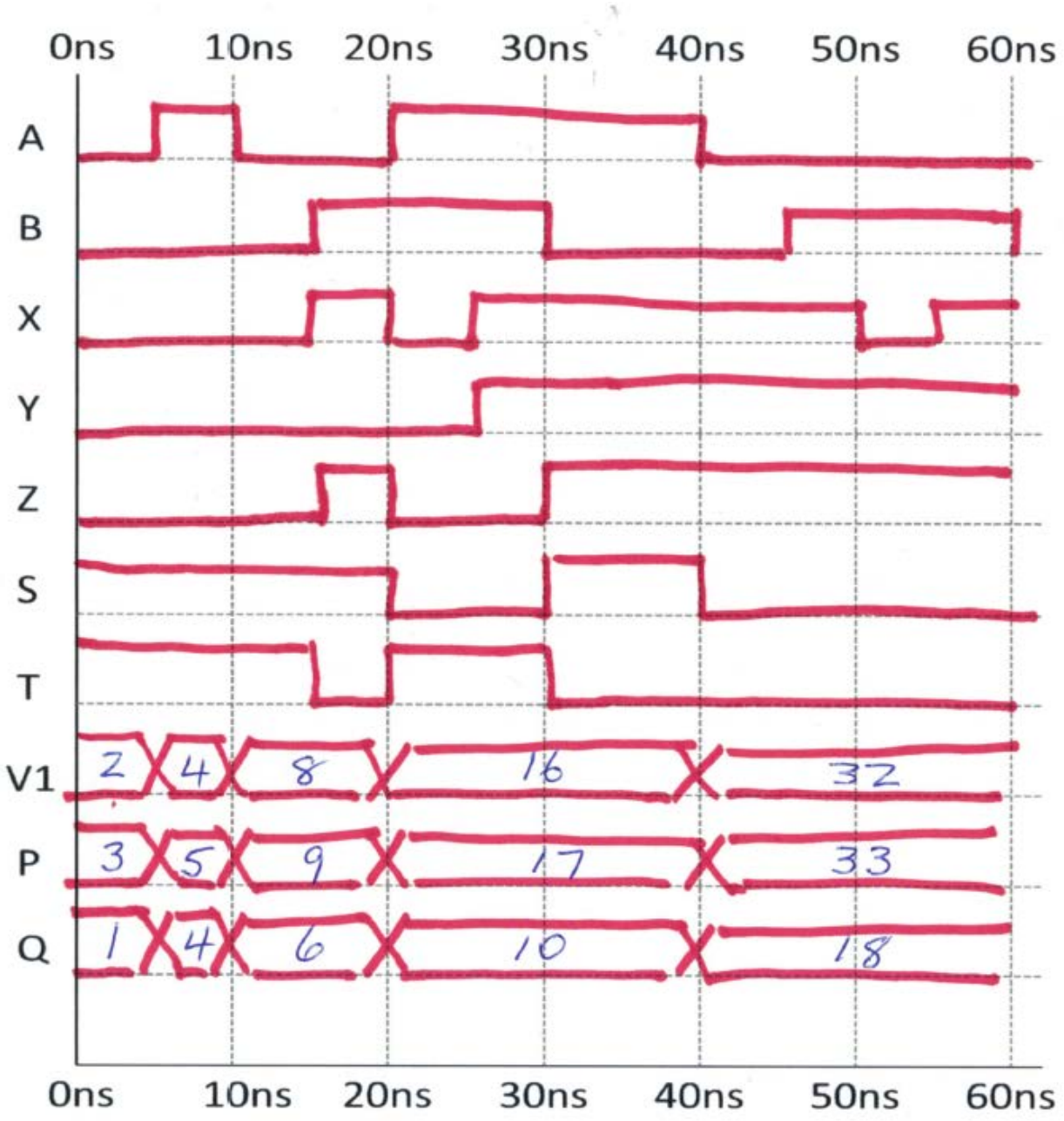
HW4 Solutions 1(b)

```
   --Inputs
   signal din : std_logic_vector(7 downto 0) := (others => '0');
   signal clk : std_logic := '0';

   --Outputs
   signal dout : std_logic_vector(7 downto 0);


type TD is array (1 to 10) of std_logic_vector(7 downto 0);
signal test_data: TD := (X"00", X"01", X"05", X"14", X"76", X"FF", X"F5", X"C3", X"CC", X"86");

BEGIN

   -- Instantiate the Unit Under Test (UUT)
   uut: twos_comp PORT MAP (
          din => din,
          clk => clk,
          dout => dout
        );



   -- Stimulus process
   stim_proc: process
   begin
      for i in 1 to 10 loop
         din <= test_data(i);
         clk <= '0', '1' after 5 ns;
         wait for 10 ns;
      end loop;
   end process;

END;
```

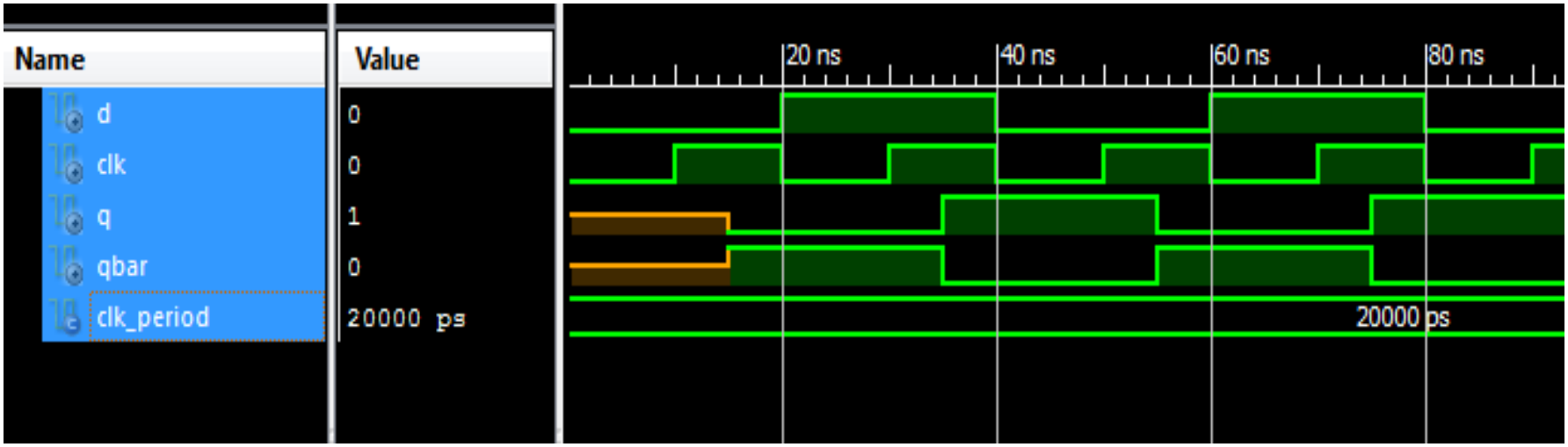
HW4 Solutions 1(b)



HW4 Solutions 2



HW4 Solutions 3(b)



HW4 Solutions 3(b)

```
entity SR4 is
    Port ( clk : in  STD_LOGIC;
           sin : in  STD_LOGIC;
           ZERO: out STD_LOGIC;
           SR : out  STD_LOGIC_VECTOR (3 downto 0));
end SR4;

architecture Structural of SR4 is

component dff is
   port(D,clk: in std_logic;
      Q,Qbar: out std_logic);
end component;
signal S0, S1, S2, S3: std_logic;
begin
D0: dff port map(D=>sin, clk=>clk, Q=>S0, Qbar=>open);
D1: dff port map(D=>S0, clk=>clk, Q=>S1, Qbar=>open);
D2: dff port map(D=>S1, clk=>clk, Q=>S2, Qbar=>open);
D3: dff port map(D=>S2, clk=>clk, Q=>S3, Qbar=>open);

ZERO <= NOT(S0 OR S1 OR S2 OR S3);

SR(3)<=S3;
SR(2)<=S2;
SR(1)<=S1;
SR(0)<=S0;
end Structural;
```

HW4 Solutions 3(b)