CPE 487: Digital System Design

Spring 2018

Lecture 0

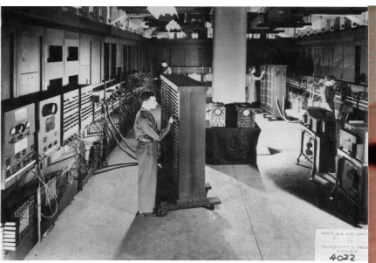
Course Organization & Introduction

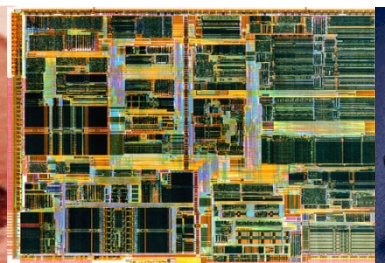
Bryan Ackland

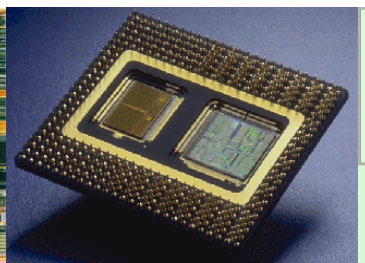
Department of Electrical and Computer Engineering

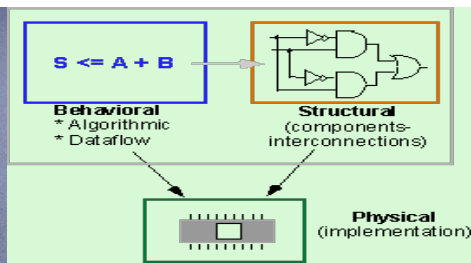
Stevens Institute of Technology

Hoboken, NJ 07030









Course Organization

- Course instructor:

  Prof. Bryan Ackland

  Office: Burchard 211

  Email: backland@stevens.edu

  Phone: (201) 216-8096

- Laboratory work:

  TA: Cong Shi

  Office: Burchard 200

  Email: cshi5@stevens.edu

  Labs held in B123

- Course web site:

http://personal.stevens.edu/~backland/Courses/Course487_Spring_18.htm

- Will use Canvas for Announcements and Gradebook only

Course Organization

- Course schedule:

  Wednesday 12:00 pm – 12:50 pm: Carnegie 316
  Friday 10:00 am – 11:40 am: Carnegie 316
  January 17 – May 3

- Office Hours:

  Wednesday 9:30 am – 11:30 am
  Thursday 10:00 am – 12:00 noon

  Other times by appointment (or just drop by)

Grading & Exam Info

- Grading Information

  -- Attendance (5%)

  -- Midterm examination (25%)

  -- Homework (20%)

  -- Laboratory Assignments (20%)

  -- Final examination (30%)

  Up to 2 grade points will be given to students who participate in class

- Exam times:

  Midterm: Friday, March 9: 10:00 am

  Final: *to be announced*

- Students may use course notes & text book during exams

Homeworks & Project

- Students are allowed to discuss assignments and collaborate on best approach to solve problems.
- Once discussion has taken place, each student must individually prepare his/her own assignment submission
- Is it OK to:
  - ask a fellow student for help in understanding how to attack a problem? YES
  - get together with a group of 2-3 colleagues and share ideas on how to approach problems? YES
  - copy another student's answers? NO
  - work with another student(s) to prepare a group solution which each submit independently? NO

Textbook & References

Textbook:

(1) *VHDL - A Starter's Guide*, Second Edition, Sudhakar Yalamanchili, Publisher: Prentice Hall, ISBN: 0-13-145735-7, 2005.

or

(2) *Introductory VHDL – From Simulation to Synthesis*, Sudhakar Yalamanchili, Publisher: Prentice Hall, ISBN 0-13-080982-9, 2001.

Recommended references:

(1) *A VHDL Primer,* 3rd edition, J. Bhasker, Prentice Hall, ISBN 0-13-096575-8, 1999.

(2) *Circuit Design with VHDL,* Volnei A. Pedroni, MIT Press, ISBN: 0-262-16224-5, 2004.

Course Objectives & Outline

Objectives:

Please visit the web site for detailed course objectives

Outlines:

- Logic gates & storage elements
- VHDL language elements
- Dataflow modeling
- Behavioral modeling
- Structural modeling
- VHDL subprograms & overloading
- Computer-aided synthesis and implementation
- Design of arithmetic logic unit (ALU)
- Finite state machines (FSM)
- Test bench design

Course Objectives & Outline

These lectures notes are based on the following sources:

[1] S. Yalamanchili, Introductory VHDL: From Simulation to Synthesis, Prentice Hall, ISBN 0-13-080982-9, 2001.

[2] S. Yalamanchili, VHDL: A Starter's Guide,, Prentice Hall, ISBN: 0-13-145735-7, 2005.

[3] J. Bhasker, A VHDL Primer,3rd edition, J. Bhasker, Prentice Hall, ISBN 0-13-096575-8, 1999

[4] S. Tewksbury, VHDL class notes

[5] Haibo He, VHDL class notes

[6] V. A. Pedroni, Circuit Design with VHDL,, MIT Press, ISBN: 0-262-16224-5, 2004.

[7] J. M. Rabaey, A. Chandrakasan, B. Nikolic, Digital integrated circuits- a design perspective, 2nd edition, prentice hall.