Introduction to VLSI Design – CPE 690

School of Engineering and Science

Meeting Times:	See Canvas
Instructor:	Prof. Bryan Ackland
Contact Info:	Burchard 211, backland@stevens.edu, (201) 216-8096
Office Hours:	See Canvas
	Other times by appt. or just stop by my office
Course Web:	Canvas
Prerequisite(s):	None formal, but see below
Corequisite(s):	None
Cross-listed with:	MT 690, PEP 690

COURSE DESCRIPTION

This course provides a general understanding of digital VLSI design. Emphasis is on transistor-level (full custom) VLSI design. Specific topics discussed in this course include the VLSI manufacturing process, design metrics, physical layout, simulation analysis, stick diagram design, MOS devices, CMOS inverter and logic gate design, static and dynamic logic, power distribution and consumption and timing analysis. Students will complete a design project in which they will use Tanner VLSI design tools to layout, extract and simulate a small digital design of their choosing. This course will also briefly introduce hardware description language (VHDL) based design using Xilinx tools to model and simulate digital circuits.

PREREQUISITES

This course presumes an undergraduate knowledge of simple electronic circuit components (resistors, capacitors, MOS transistors, voltage and current sources) and their interconnection in simple series and parallel circuit configurations. It also presumes a knowledge of Boolean digital logic functions, gates and operators (e.g. multiplexers, latches, flip-flops, adders) and two's complement binary arithmetic.

LEARNING OBJECTIVES

After successful completion of this course, students will …

- Know how to use a hardware description language (VHDL) to design, model and test complex digital circuits for implementation in FPGA or ASIC standard cell technologies.
- Be able to use commercial CAD tools to simulate and verify the correct operation of digital circuits modeled using a hardware description language (VHDL)
- Be able to develop transistor level circuit diagrams for CMOS digital gates, storage components and arithmetic operators and be able to estimate their performance
- Understand the operation of the MOS transistor and its application to CMOS digital design and understand the tradeoffs between performance, noise margin and power dissipation

- Know how to use CAD tools to layout full custom CMOS circuits obeying process design rules and evaluate the function and performance of these circuits using commercially available circuit simulation tools (SPICE)
- Understand the CMOS fabrication process and the relationship between layout and mask based fabrication.
- Know how to design transistor-level digital circuits using a number of different circuit techniques including static compound, pseudo-NMOS and dynamic gates and understand the tradeoffs in performance, area and power dissipation.

FORMAT AND STRUCTURE

This course is comprised of one lecture (150 minutes) per week.

COURSE MATERIALS

Textbook(s): CMOS VLSI Design: A Circuits and Systems Perspective (4th Edition), Neil Weste and David Harris, Publisher: Addison Wesley, ISBN: 0-321-54774-8, 2010.

Other Ref: (1) Introductory VHDL – From Simulation to Synthesis, Sudhakar Yalamanchili, Prentice Hall, ISBN: 0-13-080982-9, 2001.

(2) CMOS: Circuit Design, Layout and Simulation (2nd Edition), R. Jacob Baker, Wiley-Interscience, ISBN: 0-471-70055-X, 2005.

Materials: Stand-alone scientific calculator

COURSE REQUIREMENTS

Participation Up to (2) grade points bonus will be awarded to students who participate by frequently asking and answering questions in class

Homework There are usually seven (7) homework assignments throughout the course. All assignments count equally towards 20% of the final grade. All assignments should be submitted on the due date during class to the professor via hard copy. Homework assignments will be graded and returned within two class periods.

Project Students will complete a project of their own choosing in which they design a small full-custom digital circuit using commercial CAD tools. This includes circuit schematics, physical layout, design rule check, circuit extraction and simulation to verify function and performance over a range of temperatures and voltages using the circuit simulator SPICE. The project is graded according to difficulty of the project, accuracy of the results and quality of the presentation.

Exams There will be two exams in this course; a midterm and a final. The final exam is cumulative. The midterm will be taken in class according to the published class schedule. The final exam will normally take place during exam week; the time and place will be determined by the Registrar.

GRADING PROCEDURES

Grades will be based on:

Homework	(20 %)
Project	(20 %)
Midterm	(30 %)
Final	(30 %)

ACADEMIC INTEGRITY

All Stevens graduate students promise to be fully truthful and avoid dishonesty, fraud, misrepresentation, and deceit of any type in relation to their academic work. A student's submission of work for academic credit indicates that the work is the student's own. All outside assistance must be acknowledged. Any student who violates this code or who knowingly assists another student in violating this code shall be subject to discipline.

All graduate students are bound to the Graduate Student Code of Academic Integrity by enrollment in graduate coursework at Stevens. It is the responsibility of each graduate student to understand and adhere to the Graduate Student Code of Academic Integrity. More information including types of violations, the process for handling perceived violations, and types of sanctions can be found at www.stevens.edu/provost/graduate-academics.

EXAM ROOM CONDITIONS

The following procedures apply to exams for this course. As the instructor, I reserve the right to modify any conditions set forth below by printing revised Exam Room Conditions on the exam.

1. Students may use the following devices during exams. Any electronic devices that are not mentioned in the list below are not permitted.

Device	**Permitted?**	
	Yes	No
Laptops		X
Cell Phones		X
Tablets		X
Smart Watches		X
Google Glass		X
Stand-alone calculator	X	

2. Students may use the following materials during exams. Any materials that are not mentioned in the list below are not permitted.

Material	**Permitted?**	
	Yes	No
Handwritten Notes	X	
Typed Notes	X	
Textbooks	X	
Other reference books	X	

3. Students are not allowed to work with or talk to other students during exams.

LEARNING ACCOMODATIONS

Stevens Institute of Technology is dedicated to providing appropriate accommodations to students with documented disabilities. Student Counseling and Disability Services works with undergraduate and graduate students with learning disabilities, attention deficit-hyperactivity disorders, physical disabilities,

sensory impairments, and psychiatric disorders in order to help students achieve their academic and personal potential. They facilitate equal access to the educational programs and opportunities offered at Stevens and coordinate reasonable accommodations for eligible students. These services are designed to encourage independence and self-advocacy with support from SCDS staff. The SCDS staff will facilitate the provision of accommodations on a case-by-case basis. These academic accommodations are provided at no cost to the student.

Disability Services Confidentiality Policy

Student Disability Files are kept separate from academic files and are stored in a secure location within the office of Student Counseling, Psychological & Disability Services. The Family Educational Rights Privacy Act (FERPA, 20 U.S.C. 1232g; 34CFR, Part 99) regulates disclosure of disability documentation and records maintained by Stevens Disability Services. According to this act, prior written consent by the student is required before our Disability Services office may release disability documentation or records to anyone. An exception is made in unusual circumstances, such as the case of health and safety emergencies.

For more information about Disability Services and the process to receive accommodations, visit https://www.stevens.edu/sit/counseling/disability-services. If you have any questions please contact:

> Lauren Poleyeff, Psy.M., LCSW - Disability Services Coordinator and Staff Clinician in Student Counseling and Disability Services at Stevens Institute of Technology at lpoleyef@stevens.edu or by phone (201) 216-8728.

INCLUSIVITY STATEMENT

Stevens Institute of Technology believes that diversity and inclusiveness are essential to excellence in education and innovation. Our community represents a rich variety of backgrounds, experiences, demographics and perspectives and Stevens is committed to fostering a learning environment where every individual is respected and engaged. To facilitate a dynamic and inclusive educational experience, we ask all members of the community to:

- be open to the perspectives of others
- appreciate the uniqueness their colleagues
- take advantage of the opportunity to learn from each other
- exchange experiences, values and beliefs
- communicate in a respectful manner
- be aware of individuals who are marginalized and involve them
- keep confidential discussions private

TYPICAL COURSE SCHEDULE

(Go to Canvas Modules page for exact schedule and homework due dates)

Week	Topic(s)	Notes	Homeworks
1	Class organization Introduction to VLSI Design	Lecture 0 Lecture 1	
2	VHDL Design: Entities, Architectures & Signals Dataflow Modeling	Lecture 2	HW1
3	VHDL Design: Behavioral and Structural Modeling Subprograms & Overloading	Lecture 3	HW2
4	VHDL Design: Synthesis and Finite State Machines Test Bench Design	Lecture 4	

5	MOS Transistors and CMOS Logic	Lecture 5	HW3
6	CMOS Fabrication & Layout	Lecture 6	HW4 Design Project
7	Transistor Theory and DC Response	Lecture 7	HW5
8	Delay and Transient Response	Lecture 8	
9	Midterm Exam		
10	SPICE Simulation Logical Effort and Multi-Stage Logic Network Design	Lecture 9 Lecture 10	HW6
11	Combinational Circuit Families: Pseudo-NMOS and Dynamic Logic	Lecture 11	
12	Design for Low Power	Lecture 12	HW7
13	Design of Arithmetic Circuits	Lecture 13	
14	Final Review		
15	Final Exam		