

## Bryan Ackland – Publications

1. Åberg, I., Ackland, B., Beach, J., Godek, C., Johnson, R., King, C., Lattes, A., O'Neill, J., Pappas, S., Sriram, T. and Rafferty, C. “A Low Dark Current and High Quantum Efficiency Monolithic Germanium-on-Silicon CMOS Imager Technology for Day and Night Imaging Applications”, *IEEE International Electron Device Meeting*, San Francisco CA, Dec. 2010.
2. Rafferty, C., King, C., Ackland, B., Sproul, J., Aberg, I., O'Neill, J., Sriram, T., Godek, C., Lattes, A., Pappas, S., Buck, A. and Jovanovic, V. “Wide-band Imaging for Enhanced Day and Night Vision”, *SPIE Defense, Security & Sensing*, Orlando FL, Apr. 2010, Vol. 7660, No. 19.
3. Ackland, B., Rafferty, C., King, C., Aberg, I., O'Neill, J., Sriram, T., Lattes, A., Godek, C. and Pappas, S. “A Monolithic Ge-on-Si CMOS Imager for Short Wave Infrared”, *International Image Sensor Workshop*, Bergen, Norway, June 2009. <http://www.imagesensors.org>
4. Rafferty, C., King, C., Ackland, B., Aberg, I., Sriram, T. and O'Neill, J. “Monolithic Germanium SWIR Imaging Array”, *SPIE Defense & Security Symposium*, Orlando FL, Apr. 2008, Vol. 6940, No. 20.
5. Ackland, B., Razavi, B. and West, L. “A Comparison of Electrical and Optical Clock Networks in Nanometer Technologies”, *IEEE Custom Integrated Circuits Conference*, San Jose CA, Sept. 2005, pp.779-782.
6. Ackland, B., “Systems on a Chip for a Battered Communications IC Market”, *IEEE Intl. Symposium on VLSI Technology, Systems & Applications*, Hsinchu Taiwan, Oct. 2003. [Invited Keynote]
7. Williams, J., Ackland, B. and Heintze, N. “Communication Mechanisms for Parallel DSP Systems on a Chip”, *Design, Automation and Test in Europe*, Paris, March 2002. pp. 420–422.
8. Ackland, B., Anesko, A., Brinthaup, D., Daubert, S.J., Kalavade, A., Knobloch, J., Micca, E., Moturi, M., Nicol, C.J., O'Neill, J.H., Othmer, J., Sackinger, E., Singh, K.J., Sweet, J., Terman, C.J., and Williams, J. “A Single-chip, 1.6-billion, 16-b MAC/s Multiprocessor DSP” *IEEE Journal Solid-State Circuits*, Vol. 35, No. 3, March 2000, pp. 412-424.
9. Williams, J., Singh, K.J., Nicol, C., Sackinger, E., Daubert, S., Micca, E., Moturi, M., Knobloch, J., Brinthaup, D. and Ackland, B. “A 3.2 GOPS Multiprocessor DSP for Communication Applications” *IEEE Solid-State Circuits Conference*, San Francisco CA Feb. 2000. pp. 70 –71.
10. Svensson, C., Soumyanath, K., Kaiser, B., Vasudev, P., Kalter, H. and Ackland, B., “RF Integration into CMOS and Deep Sub-micron Challenges”, *IEEE Design and Test of Computers*, Vol. 16 No. 3, Jul-Sep 1999, pp. 112-116.
11. Kalavade, A., Othmer, J., Ackland, B., and Singh, K. “Software Environment for a Multiprocessor DSP”, *IEEE/ACM Design Automation Conf.*, New Orleans LA, June 1999, pp. 827-830.
12. Ackland, B. and D'Arcy, P. “A New Generation of DSP Architectures”, *IEEE Custom Integrated Circuits Conference*, San Diego CA, May 1999, pp. 531-536.
13. Ackland, B., Anesko, A., Brinthaup, D., Daubert, S., Kalavade, A., Knobloch, J., Micca, E., Moturi, M., Nicol, C., O'Neill, J., Othmer, J., Sackinger, E., Singh, K., Sweey, J., Terman, C. and Williams, J. “A Single Chip 1.6 Billion 16-b MAC/s Multiprocessor DSP”, *IEEE Custom Integrated Circuits Conference*, San Diego CA, May 1999, pp. 537-540.
14. Loinaz, M., Singh, K., Blanksby, A., Inglis, D., Azadet, K. and Ackland, B. “A 200 mW, 3.3V CMOS Color Camera IC Producing 352x288 24b Video at 30 Frames/s” *IEEE Journal Solid State Circuits*, Vol. 33, No. 12, Dec. 1998, pp. 2092-2103.
15. Ackland, B. and Nicol, C. “High Performance DSP's: What's Hot and What's Not?” *International Symp. On Low Power Electronics and Design*, Monterey CA, Aug. 1998, pp. 1-6. [Invited Keynote]

16. Loinaz, M., Singh, K., Blanksby, A., Inglis, D., Azadet, K. and Ackland, B. "A 200 mW, 3.3V CMOS Color Camera IC Producing 352x288 24b Video at 30 Frames/s", *IEEE International Solid State Circuits Conf.*, San Francisco CA, Feb. 1998, pp. 168-169.
17. Inglis, D., Manchanda, L., Comizzoli, R., Dickinson, A., Martin, E., Mendis, S., Silverman, P., Weber, G., Ackland, B. and O'Gorman, L. "A Robust 1.8V 250mW Direct-Contact 500 dpi Fingerprint Sensor", *IEEE International Solid State Circuits Conf.*, San Fransisco CA, Feb. 1998, pp. 284-285.
18. Blanksby, A., Loinaz, M., Inglis, D. and Ackland, B. "Noise Performance of a Color CMOS Photogate Image Sensor", *IEEE International Electron Devices Meeting*, Washington D.C., Dec. 1997 pp. 205-208.
19. Ackland, B. "Programmable Multimedia Signal Processors" in *Circuits and Systems for the Information Age*, edited by Y-Y Huang and C-H Wei, IEEE Press, 1997.
20. Ackland, B. and Dickinson, A., "A Single Chip CMOS Camera," Plenary Presentation, *IEEE Intl. Solid State Circuits Conf.*, San Francisco CA, Feb. 1996, pp. 22-25.
21. Jayant, N., Ackland, B., Lawrence, V. and Rabiner, L., "Multimedia: Technology Dimensions and Challenges", *AT&T Technical Journal*, Vol. 74, No. 5, September 1995, pp. 14-33.
22. Dickinson, A., Ackland, B., Eid, E., Inglis, D. and Fossum, E., "Standard CMOS Active Pixel Image Sensors for Multimedia Applications, *Sixteenth Conference on Advanced Research in VLSI*, Chapel Hill NC, March 1995, pp. 214-224.
23. Dickinson, A., Ackland, B., Eid, E., Inglis, D., and Fossum, E., "A 256x256 CMOS Active Pixel Image Sensor with Motion Detection", *IEEE Intl. Solid State Circuits Conf.*, San Francisco CA, Feb. 1995, pp. 226-227.
24. Eid, E., Dickinson, A., Inglis, D., Ackland, B. and Fossum, E., "CMOS Active Pixel Image Sensors for Low Cost Applications", *IEEE Intl. Conf. on Electronics Circuits & Systems*, Cairo Egypt, Dec. 1994.
25. Yu, M. and Ackland, B., "VLSI Timing Simulation with Selective Regionization", *IEEE International Conf. on Computer Aided Design*, San Jose CA, Nov. 1994, pp. 195-199.
26. Ackland, B., "VLSI Architectures for Multimedia and Video Conferencing", in *Circuits & Systems Tutorials, ISCAS '94*, ed. by Chris Toumazou, LTP Electronics UK 1994.
27. Ackland, B., "The Role of VLSI in Multimedia", *IEEE Journal of Solid State Circuits*, Vol. 29, No. 4, April 1994, pp. 381-388.
28. Ackland, B., "Video Compression and VLSI," *IEEE Custom Integrated Circuits Conference*, San Diego CA, May 1993, pp. 11.1.1-11.1.6.
29. Ackland, B. "The Role of VLSI in Multimedia," *1993 Symposium on VLSI Circuits*, Kyoto Japan, May 1993, pp. 1-4.
30. O'Neill, J., Ackland, B., Rao, S. and Hatamian, M., "A 200 MHz CMOS Broadband Switching Chip", *IEEE Journal of Solid State Circuits*, Vol. 28, No. 3, March 1993, pp. 269-275.
31. Ackland, B., Aghevli, R., Eldumiati, I., Englander, A. and Scuteri, E., "A Video Codec Chip Set for Multimedia Applications, *AT&T Technical Journal*, Vol. 72, No. 1, January 1993, pp. 50-66.
32. Ackland, B., "Multimedia and VLSI," Keynote Address, *Second Australian Multimedia Communications, Applications and Technology Workshop*, Melbourne Australia, July 1992, pp. 6-7.
33. O'Neill, J., Ackland, B., Hatamian, M., Rao, S., "A 200 MHz CMOS Broadband Switching Chip," *IEEE Custom Integrated Circuits Conference*, Boston MA, May 1992, pp. 14.1.1-14.1.5

34. Rao, S., Hatamian, M. and Ackland, B., "A Design Environment for High Performance VLSI Signal Processing, *IEEE International Conf. on Computer Design*, Cambridge MA, Sept. 1990, pp. 147-152.
35. Rao, S., Hatamian, M. and Ackland, B. "A Design Environment for High Performance VLSI Signal Processing," *International Symposium on Signal Processing*, Gold Coast, Australia, Aug. 1990, pp. 630-635.
36. Ackland, B. "Knowledge Based VLSI Design Synthesis" in *VLSI and Parallel Computation*, edited by R. Suaya and G. Birtwistle, Morgan Kaufman, 1990.
37. Ackland, B. and Clark, R. "Event-EMU: An Event Driven Timing Simulator for MOS VLSI Circuits," *IEEE International Conf. on Computer Aided Design*, Santa Clara CA, Nov. 1989, pp. 80-83.
38. Director, S., Ackland, B., Joobbani, R., Sangiovanni-Vincentelli, A., Smith, R. and Steele R., "A D&T Roundtable – Expert Systems in CAD", *IEEE Design and Test of Computers*, Vol. 6 No. 4, Aug. 1989, pp. 61-68.
39. Ackland, B. "Experiences with Advanced Design Automation Tools," *IFIP 11th. World Congress*, San Francisco, CA, Aug. 1989, p. 532.
40. Ackland, B., "Knowledge Based Physical Design Automation", in *Physical Design Automation of VLSI Systems*, ed. by B. Preas & M. Lorenzetti, Benjamin Cummins 1988, pp. 409-460.
41. Kravitz S. and Ackland, B."Static vs. Dynamic Partitioning of Circuits for a MOS Timing Simulator on a Message Based Multiprocessor," *SCS Multiconference on Distributed Simulation*, San Diego CA, Feb. 1988, pp. 136-140.
42. DeBenedictis, E. and Ackland, B., "Circuit Simulation on a Hypercube. *SCS Multiconference on Distributed Simulation*, San Diego CA, Feb. 1988, pp. 89-93.
43. Watanabe, H. and Ackland, B., "FLUTE: An Expert Floorplanner for Full Custom VLSI Design", *IEEE Design and Test*, Feb. 1987, pp. 32-41.
44. Ackland, B. *et al.* "MOS Timing Simulation on a Message Based Multiprocessor," *IEEE International Conf. on Computer Design*, Port Chester NY, Oct. 1986, pp. 446-450.
45. Kollaritsch, P. and Ackland, B., "Coordinator: A Complete Design Rule Enforced Layout Methodology", *IEEE International Conf. on Computer Design*, Port Chester NY, Oct. 1986, pp. 302-307.
46. Watanabe, H. and Ackland, B. "Flute - A Floorplanning Agent for Full Custom VLSI Design", *23rd. Design Automation Conference*, Las Vegas NV, June 1986, pp. 601-607.
47. Ackland, B., Ahuja, S., Lindstrom, T. and Romero, D., "CEMU - A Concurrent Timing Simulator," *IEEE International Conf. on Computer-Aided Design*, Santa Clara CA, Nov. 1985, pp. 122-124.
48. Ackland, B. *et al.* "CADRE - A System of Cooperating VLSI Design Experts", *IEEE International Conf. on Computer Design: VLSI in Computers*, Port Chester NY, Oct. 1985, pp. 99-104.
49. Ackland, B., "Dynamic Time Warp Processor", in *Principles of CMOS VLSI Design*, N. Weste and K. Eshragian, Addison Wesley 1985, pp. 384-406.
50. Burr, D., Ackland, B. and Weste, N. "Array Configurations for Dynamic Time Warping", *IEEE Trans. on Acoustics, Speech and Signal Processing*, Vol. 32, No. 1, Feb. 1984, pp. 119-128.
51. Weste, N., Burr, D. and Ackland, B., "Dynamic Time Warp Pattern Matching Using an Integrated Multiprocessing Array", *IEEE Trans. on Computers*, Vol. 32, No. 8, Aug. 1983, pp. 731-744.
52. Ackland, B. and Weste, N., "An Automatic Assembly Tool for Virtual Grid Symbolic Layout." *VLSI '83*, Trondheim Norway, Aug. 1983, pp. 457-466.

53. Ackland, B. and Weste, N., "A Pragmatic Approach to Topological Symbolic IC Design." *Microelectronics '82*, The Institution of Engineers, Australia. Adelaide, Aust. May 1982, pp. 27-31.
54. Weste, N., Burr, D. and Ackland, B., "A Systolic Processing Element for Speech Recognition." *IEEE International Solid-State Circuits Conf.*, San Francisco CA, Feb. 1982, pp. 274-275.
55. Ackland, B. and Weste, N., "Color Display Terminals for VLSI: Another Perspective." *VLSI Design*, Vol. 3, No. 1, Jan./Feb. 1982, pp. 56-59.
56. Weste, N. and Ackland, B., "A Pragmatic Approach to Topological Symbolic IC Design." *1st. International Conf. on VLSI*, Edinburgh UK, Aug. 1981, pp. 117-129.
57. Ackland, B., Weste, N. and Burr, D., "An Integrated Multiprocessing Array for Time Warp Pattern Matching", *8th. IEEE Symp. on Computer Architecture*, Minneapolis MN, May 1981, pp. 197-214.
58. Burr, D., Ackland, B. and Weste, N., "A High-Speed Array Computer for Dynamic Time Warping", *IEEE International Conf. on Acoustics, Speech and Signal Processing*, Atlanta GA, March 1981, pp. 471-474.
59. Ackland, B. and Weste, N., "The Edge-Flag Algorithm - A Fill Method for Raster Scan Displays", *IEEE Trans. on Computers*, Vol. 30, No. 1, Jan. 1981, pp. 41-48.
60. Ackland, B. and Weste, N., "Functional Verification in an Interactive Symbolic IC Design Environment", *Second Caltech Conf. on VLSI*, Jan. 1981, pp. 285-298.
61. Ackland, B. and Weste, N., "Real Time Animation Playback on a Frame Store Display System", *ACM SIGGRAPH '80*, Seattle WA., July 1980, pp. 182-188.
62. Weste, N. and Ackland, B., "An IC Design Station Needs a High Performance Color Graphic Display", *IEEE/ACM Design Automation Conf.*, Minneapolis MN., June 1980, pp. 285-291.
63. Weste, N. and Ackland, B., "GUMBI - A Graphic User Microprogrammable Bit-Slice Interpreter", *IEEE Compcon Fall 79*, Washington DC., Sept. 1979, pp. 232-237.
64. Ackland, B., "A Bit-Slice Cache Controller", *IEEE/ACM 6th. Annual Symp. on Computer Architecture*, Philadelphia, PA., April 1979, pp. 75-82.
65. Fensom, D.S., Smith, N.I. and Ackland, B., "GASP - a Fast General Purpose Signal Processor." *Conf. on Computers in Engineering*, The Institution of Engineers, Australia. Canberra, Aust., Aug. 1978, pp. 81-86.
66. Ackland, B. and Weste, N., "A Microprocessor Based Home Terminal", *Colloq. on Microprocessor Systems*, The Institution of Engineers, Australia, Sydney, Aust., Nov. 1976, pp. 11-12.
67. Ackland, B. and Pucknell, D., "Cache Store Concepts in Real-Time Engineering Minicomputer Systems", *Conf. on Computers in Engineering*, The Institution of Engineers, Australia. Perth, Aust., Sept. 1976, pp. 120-124.
68. Ackland, B. and Pucknell, D., "Studies of Cache Store Behavior in a Real-Time Minicomputer Environment", *Electronics Letters*, 1975, Vol. II, No. 24, pp. 588-590.

### **Granted Patents:**

1. **8,686,365** “Imaging Apparatus and Methods”, April 2014.
2. **8,648,948** “Imaging Systems with Multiple Imaging Pixel Types and Related Methods”, Feb. 2014.
3. **8,634,008** “Image Signal Processing Methods and Apparatus”, Jan. 2014.
4. **8,586,907** “Methods of Operating an Imaging Pixel to Accumulate Charge from a Photocurrent”, Nov. 2013.
5. **8,294,100** “Imaging Apparatus and Methods”, Oct. 2012.
6. **8,084,739** “Imaging Apparatus and Methods”, Dec. 2011.
7. **8,072,525** “Imaging Signal Processing Methods and Apparatus”, Dec. 2011.
8. **8,063,422** “Image Detection Apparatus and Methods”, Nov. 2011.
9. **8,022,350** “Imaging Pixel Comprising a Comparator to Compare Integrated Photocurrent to a Reference Value and Digital Output Circuitry”, Sept 2011.
10. **7,528,357** “Pulse detector which employs a self-resetting pulse amplifier”, May 2009.
11. **7,326,903** “Mixed analog and digital pixel for high dynamic range readout”, Feb. 2008.
12. **6,150,922** “Serial Communication Technique”, Nov. 2000
13. **6,141,050** “MOS Image Sensor”, Oct., 2000
14. **6,097,195** “Methods and Apparatus for Increasing Metal Density in an Integrated Circuit while also Reducing Parasitic Capacitances”. Aug., 2000
15. **5,987,156** “Apparatus for Correcting Fixed Column Noise in Images Acquired By A Fingerprint Sensor”, Nov., 1999
16. **5,835,141** “Single Polysilicon CMOS Active Pixel Image Sensor, Oct., 1998
17. **5,739,562** “Combined photogate and photodiode active pixel image sensor”, April 1998
18. **5,604,705** “Static random access memory sense amplifier”, Feb. 1997
19. **5,576,763** “Single-Polysilicon CMOS Active Pixel,” Nov. 1996
20. **5,541,402** “Imaging Active Pixel Device Having A Non-Destructive Read-Out Gate”, July 1996
21. **5,220,325** “Hierarchical Variable Length Decoder for Digital Video Data,” June 1993
22. **4,509,187** “Time Warp Signal Recognition Processor Using Recirculating and/or Reduced Array of Processor Cells,” May 1985.
23. **4,412,313** “Random Memory Access System Having High-Speed Serial Data Paths,” Oct. 1983.
24. **4,384,273** “Time Warp Signal Recognition Processor for Matching Signal Patterns,” May 1983

### **Published Patent Applications:**

1. **20100019154** “Imaging Apparatus and Methods”, Jan. 2010.
2. **20070127922** “Eliminating Clock Skew by using Bidirectional Signaling”, June 2007
3. **20070127615** “DC Technique for Eliminating Phase Ambiguity in Clocking Signals”, June 2007
4. **20060055800** “Imaging Apparatus and Methods”, Mar. 2006