Memory and Advanced Digital Circuits
Chapter 11
Figure 11.1 (a) Basic latch. (b) The latch with the feedback loop opened. (c) Determining the operating point(s) of the latch.
Figure 11.2 (a) The set/reset (SR) flip-flop and (b) its truth table.

<table>
<thead>
<tr>
<th>$R$</th>
<th>$S$</th>
<th>$Q_{n+1}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>$Q_n$</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>Not used</td>
</tr>
</tbody>
</table>
Figure 11.3 CMOS implementation of a clocked SR flip-flop. The clock signal is denoted by $\phi$. 

![CMOS implementation of a clocked SR flip-flop](image_url)
Figure 11.4 The relevant portion of the flip-flop circuit of Fig. 11.3 for determining the minimum $W/L$ ratios of $Q_5$ and $Q_6$ needed to ensure that the flip-flop will switch.
Figure 11.5 A simpler CMOS implementation of the clocked SR flip-flop. This circuit is popular as the basic cell in the design of static random-access memory (SRAM) chips.
Figure 11.6  A block-diagram representation of the D flip-flop.
Figure 11.7 A simple implementation of the D flip-flop. The circuit in (a) utilizes the two-phase nonoverlapping clock whose waveforms are shown in (b).
Figure 11.8 (a) A master–slave D flip-flop. The switches can be, and usually are, implemented with CMOS transmission gates. (b) Waveforms of the two-phase nonoverlapping clock required.
Figure 11.9 The monostable multivibrator (one-shot) as a functional block, shown to be triggered by a positive pulse. In addition, there are one shots that are triggered by a negative pulse.
Figure 11.10  A monostable circuit using CMOS NOR gates. Signal source $v_I$ supplies positive trigger pulses.
Figure 11.11 (a) Diodes at each input of a two-input CMOS gate. (b) Equivalent diode circuit when the two inputs of the gate are joined together. Note that the diodes are intended to protect the device gates from potentially destructive overvoltages due to static charge accumulation.
Figure 11.12 Output equivalent circuit of CMOS gate when the output is (a) low and (b) high.
Figure 11.13 Timing diagram for the monostable circuit in Fig. 11.10.
Figure 11.14 Circuit that applies during the discharge of $C$ (at the end of the monostable pulse interval $T$).
Figure 11.15  (a) A simple astable multivibrator circuit using CMOS gates. (b) Waveforms for the astable circuit in (a). The diodes at the gate input are assumed to be ideal and thus to limit the voltage $v_{i_1}$ to 0 and $V_{DD}$. 
Figure 11.16 (a) A ring oscillator formed by connecting three inverters in cascade. (Normally at least five inverters are used.) (b) The resulting waveform. Observe that the circuit oscillates with frequency $1/6t_p$. 
Figure 11.17 A $2^M \times 2^N$-bit memory chip organized as an array of $2^M$ rows $\times 2^N$ columns.
Figure 11.18 A CMOS SRAM memory cell.
Figure 11.19 Relevant parts of the SRAM cell circuit during a read operation when the cell is storing a logic 1. Note that initially $v_Q = V_{DD}$ and $v_{\bar{Q}} = 0$. Also note that the $B$ and $\bar{B}$ lines are usually precharged to a voltage of about $V_{DD}/2$. However, in Example 11.2, it is assumed for simplicity that the precharge voltage is $V_{DD}$. 
Figure 11.20 Relevant parts of the SRAM circuit during a write operation. Initially, the SRAM has a stored 1 and a 0 is being written. These equivalent circuits apply before switching takes place. (a) The circuit is pulling node $\bar{Q}$ up toward $V_{DD}/2$. (b) The circuit is pulling node $Q$ down toward $V_{DD}/2$. 
Figure 11.21 The one-transistor dynamic RAM cell.
When the voltage of the selected word line is raised, the transistor conducts, thus connecting the storage capacitor $C_S$ to the bit-line capacitance $C_B$. 

Figure 11.22
Figure 11.23 A differential sense amplifier connected to the bit lines of a particular column. This arrangement can be used directly for SRAMs (which utilize both the $B$ and $\overline{B}$ lines). DRAMs can be turned into differential circuits by using the “dummy cell” arrangement shown in Fig. 11.25.
Figure 11.24 Waveforms of $v_B$ before and after the activation of the sense amplifier. In a read-1 operation, the sense amplifier causes the initial small increment $\Delta V(1)$ to grow exponentially to $V_{DD}$. In a read-0 operation, the negative $\Delta V(0)$ grows to 0. Complementary signal waveforms develop on the $B$ line.
Figure 11.25 An arrangement for obtaining differential operation from the single-ended DRAM cell. Note the dummy cells at the far right and far left.
Figure 11.26 A NOR address decoder in array form. One out of eight lines (row lines) is selected using a 3-bit address.
Figure 11.27 A column decoder realized by a combination of a NOR decoder and a pass-transistor multiplexer.
Figure 11.28 A tree column decoder. Note that the colored path shows the transistors that are conducting when \( A_0 = 1, A_1 = 0, \) and \( A_2 = 1, \) the address that results in connecting \( B_3 \) to the data line.
Figure 11.29 A simple MOS ROM organized as 8 words × 4 bits.
Figure 11.30 (a) Cross section and (b) circuit symbol of the floating-gate transistor used as an EPROM cell.
Figure 11.31 Illustrating the shift in the $i_D - v_{GS}$ characteristic of a floating-gate transistor as a result of programming.
Figure 11.32 The floating-gate transistor during programming.
Figure 11.33 The basic element of ECL is the differential pair. Here, $V_R$ is a reference voltage.
Figure 11.34 Basic circuit of the ECL 10K logic-gate family.
Figure 11.35 The proper way to connect high-speed logic gates such as ECL. Properly terminating the transmission line connecting the two gates eliminates the “ringing” that would otherwise corrupt the logic signals. (See Section 11.7.6.)
Figure 11.36  Simplified version of the ECL gate for the purpose of finding transfer characteristics.
Figure 11.37 The OR transfer characteristic $v_{OR}$ versus $v_I$, for the circuit in Fig. 11.36.
Figure 11.38 Circuit for determining $V_{OH}$. 

$R_{C2} = 245 \, \Omega$

$Q_2$

$V_{OH}$

50 \, \Omega

-2 \, V
Figure 11.39 The NOR transfer characteristic, $v_{\text{NOR}}$ versus $v_I$, for the circuit in Fig. 11.36.
Figure 11.40 Circuit for finding, $v_{\text{NOR}}$ versus $v_I$ for the range $v_I > V_{\text{IH}}$. 

$R_{C1} = 220 \ \Omega$

$R_E = 779 \ \Omega$

$R_T = 50 \ \Omega$

$-5.2 \ \text{V}$

$-2 \ \text{V} (V_T)$
Figure 11.41 Equivalent circuit for determining the temperature coefficient of the reference voltage $V_R$. 
Figure 11.42 Equivalent circuit for determining the temperature coefficient of $V_{OL}$. 

$\Delta V_{OL} = R_T \delta$

$\Delta V_R = -0.7 \delta$
Figure 11.43 Equivalent circuit for determining the temperature coefficient of $V_{OH}$. 
Figure 11.44 The wired-OR capability of ECL.
Figure 11.45 Development of the BiCMOS inverter circuit. (a) The basic concept is to use an additional bipolar transistor to increase the output current drive of each of $Q_N$ and $Q_P$ of the CMOS inverter. (b) The circuit in (a) can be thought of as utilizing these composite devices.
Figure 11.45 (Continued) (c) To reduce the turn-off times of $Q_1$ and $Q_2$, “bleeder resistors” $R_1$ and $R_2$ are added. (d) Implementation of the circuit in (c) using NMOS transistors to realize the resistors. (e) An improved version of the circuit in (c) obtained by connecting the lower end of $R_1$ to the output node.
Figure 11.46 Equivalent circuits for charging and discharging a load capacitance $C$. Note that $C$ includes all the capacitances present at the output node.
Figure 11.47 A BiCMOS two-input NAND gate.
PARAMETERS:
R1 = 907
R2 = 4.98K
R3 = 6.1K
Ra = 50K
Rb = 50K
Rc1 = 220
Rc2 = 245
Re = 779

Figure 11.48 Capture schematic of the two-input ECL gate for Example 11.5.
Figure 11.49  Circuit arrangement for computing the voltage transfer characteristics of the ECL gate in Fig. 11.48.
Figure 11.50 Voltage transfer characteristics of the OR and NOR outputs (see Fig. 11.49) for the ECL gate shown in Fig. 11.48. Also indicated is the reference voltage, $V_R = -1.32 \text{ V}$. 

$v_{\text{NOR}}$ $v_{\text{OR}}$ $v_{\text{R}}$ $v_A$

Reference voltage

OR output

NOR output
Figure 11.51 Comparing the voltage transfer characteristics of the OR and NOR outputs (see Fig. 11.49) of the ECL gate shown in Fig. 11.48, with the reference voltage $V_R$ generated using: (a) the temperature-compensated bias network of Fig. 11.48.
Figure 11.51 (Continued) (b) a temperature-independent voltage source.
Figure 11.52 Circuit arrangement for investigating the dynamic operation of ECL. Two ECL gates (Fig. 11.48) are connected in cascade via a 1.5-m coaxial cable which has a characteristic impedance \( Z_0 = 50 \Omega \) and a propagation delay \( t_d = 10 \text{ ns} \). Resistor \( R_{T1} (50 \Omega) \) provides proper termination for the coaxial cable.
Figure 11.53 Transient response of a cascade of two ECL gates interconnected by a 1.5-m coaxial cable having a characteristic impedance of 50 Ω and a delay of 10 ns (see Fig. 11.52).
Figure 11.54 Transient response of a cascade of two ECL gates interconnected by a 1.5-m cable having a characteristic impedance of 300 Ω. The termination resistance $R_{T1}$ (see Fig. 11.52) was kept unchanged at 50 Ω. Note the change in time scale of the plot.
Figure P11.40