Computer and Digital System Architecture

EE/CpE-810-A

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Week 12

Embedded ARM applications

Furber Ch. 13
System-on-a-chip concept

- CPU
- MMU
- Memory
- Coprocessor(s)
- I/O Interface(s)
- Special Purpose Hardware
- Peripherals
- Memory
Ruby II advanced communication controller

- ARM core
- 512x32 SRAM
- Interrupt controller
- Counter/timer
- Clock control
- Parallel I/F 1,2,3,4
- I/O mode select
- PCMCIA host interface
- UART1 (2)
- Host FIFOs (16x8)
- Serial FIFOs (16x8)
- Serial controller
- Parallel interface 0
- External bus control
- External interrupts (3)
- Control
- Address (22)
- Data (8/16/32)
- I²C
- 8 data bits & control
- Serial
- High-speed serial I/F
Ruby II advanced communication controller

<table>
<thead>
<tr>
<th>Mode</th>
<th>Function</th>
<th>Current</th>
<th>Power</th>
</tr>
</thead>
<tbody>
<tr>
<td>On-line</td>
<td>All circuits clocked at full speed</td>
<td>30 mA</td>
<td>150 mW</td>
</tr>
<tr>
<td>Command</td>
<td>ARM core runs with 1-64 wait states, all other circuits run at full speed.</td>
<td>7.9 mA</td>
<td>40 mW</td>
</tr>
<tr>
<td></td>
<td>Interrupts cause system to change to on-line mode</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Sleep</td>
<td>Other than oscillators and timers, all circuitry stopped. Some interrupts change system to on-line mode</td>
<td>1.5 mA</td>
<td>7.5 mW</td>
</tr>
<tr>
<td>Stop</td>
<td>All circuits (including timers and oscillators) stopped. Some interrupts return system to on-line mode</td>
<td>150 μA</td>
<td>750 μW</td>
</tr>
</tbody>
</table>

Power consumption at 5V, 20 MHz

80-pin TQFP package

Ruby II available in 144 and 176-pin TQFP as standard communications processor
Typical VIP (VLSI ISDN Subscriber Processor) system configuration

- Display
- V24 interface
- S0 ISDN interface
- Driver
- Power
- ROM
- RAM
- ISDN subscriber processor
- Volume
- Hands-free
- Hook switch
- KEY
- PAD
VIP organization

36.864 MHz during normal operation

460.8 kHz during power-down

Reset if no activity for 1.28 sec

Refresh DRAM every 2.5 ms

36.864 MHz during normal operation

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Reset if no activity for 1.28 sec

Refresh DRAM every 2.5 ms
Clock generation

(1) Generating low speed clocks, e.g., 1 second signal for RTC

32.768 kHz

piezoelectric crystal oscillator

Divide by $N = 2^{15}$

1 Hz

How do you generate clocks at higher frequencies than oscillator?
Clock generation

(2) Generating high speed clocks, e.g., processor clock at 50 MHz

- System clock oscillator
- M/N PLL
- piezoelectric crystal oscillator

\[ f_{\text{ref}} \rightarrow \text{System clock oscillator} \rightarrow \text{M/N PLL} \rightarrow M/N \times f_{\text{ref}} \]
Clock generation

(2) Generating high speed clocks, e.g., processor clock at 50 MHz

\[ f_{\text{out}} = f_{\text{ref}} \times M \]
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\[ f_{out} = f_{ref} \times \frac{M}{N} \]
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Clock generation

\[ f_{out} = f_{ref} \times \frac{M}{N} \]
Typical GSM handset architecture
GSM handset power management

- Power down most circuitry (digital, analog, RF) between calls, except to periodically listen on control channel for calls
- Slow down clocks in idle mode
- Pulse-width modulate battery charging circuitry for optimum operation
- Use A/Ds to monitor battery temperature and change/discharge voltage
OneC VWS22100 GSM chip organization

- GSM protocol stack
- user interface
- power management
- peripheral I/O
- data applications

- Voice coding
- equalization
- channel coding
- echo cancellation
- noise suppression
- voice recognition
- data compression

EE810A
4/18/2011
Bluetooth networking

- Piconet master
- Piconet slaves

Ad-hoc piconet
~10 cm – 10 m range
2 – 8 stations
Common hopping sequence and synchronized clocks
Bluetooth networking

Scatternet made of multiple piconets
Typical Bluetooth application

- Flash memory
- Bluetooth baseband controller
- Radio module
- Host interface (RS232/USB)
Ericsson-VLSI Bluetooth Baseband Controller organization

**Ericsson Bluetooth Core**
- link controller
- packet handling
- radio interface
Bluetooth chip power

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<tr>
<td>On-line</td>
<td>All circuits clocked at full speed</td>
<td>30 mA</td>
<td>75 mW</td>
</tr>
<tr>
<td>Command</td>
<td>ARM7TDMI core runs with wait states,</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Sleep</td>
<td>ARM7TDMI is stopped, power state of other circuits is programmable</td>
<td>300 µA</td>
<td>750 µW</td>
</tr>
<tr>
<td>Stop</td>
<td>Clock oscillators are stopped</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Ericsson Bluetooth chip

approx. 4.5 mm
Next steps

Integration of RF circuitry with digital and processor circuits
Typical ARM7500 system organization

Functions included:

CPU
Floating point co-processor
Video and sound I/F
Memory and peripheral controller
→ nearly complete PC function

Applications
• Acorn RISC PC
• Video set top box
ARM7500 chip

approx 8.5 mm
The Psion Series 5MX PDA
The Psion Series 5 hardware organization
ARM7100 organization

- ARM710a
  - MMU
  - ARM7 core
  - 8 kbyte cache
  - LCD controller
  - interrupt controller
  - AMBA

- External bus control
  - Address (28)
  - Data (32)

- Control
- Power mgmt
- Counter/timers

- UART
- Codec I/F
- Sync serial
- Parallel I/O

- DRAM controller
  - DRA (13)
  - RAS, CAS (8)
  - WE, OE (2)

- Expansion
- PSU control

- Clock PLL
- RTC osc
- 3.6864 MHz
- 32.768 kHz
ARM7100 chip
SA-1100 organization

- CPU core
- Instruction MMU
- Instruction cache
- StrongARM core
- Data cache
- Mini-cache
- Data MMU
- Write buffer
- Read buffer
- System bus
- Memory & PCMCIA
- Serial 0
- Serial 1
- Serial 2
- Serial 3
- Serial 4
- Codec (4)
- UART (2)
- IrDA (2)
- USB (2)
- SDLC (2)
- Serial 0
- Serial 1
- Serial 2
- Serial 3
- Serial 4
- Control
- Address (26)
- Power manager
- Reset (2)
- Battery (3)
- I/O pins (28)
- 32.768 kHz
- 3.6864 MHz
- Clock PLL
- RTC oscillator
- RTC
- Interrupt control
- OS timer
- Reset control
- LCD control
- LCD (5)
SA-1100 chip

approx 9 mm