Field Programmable Interferer-Reflecting LNAs

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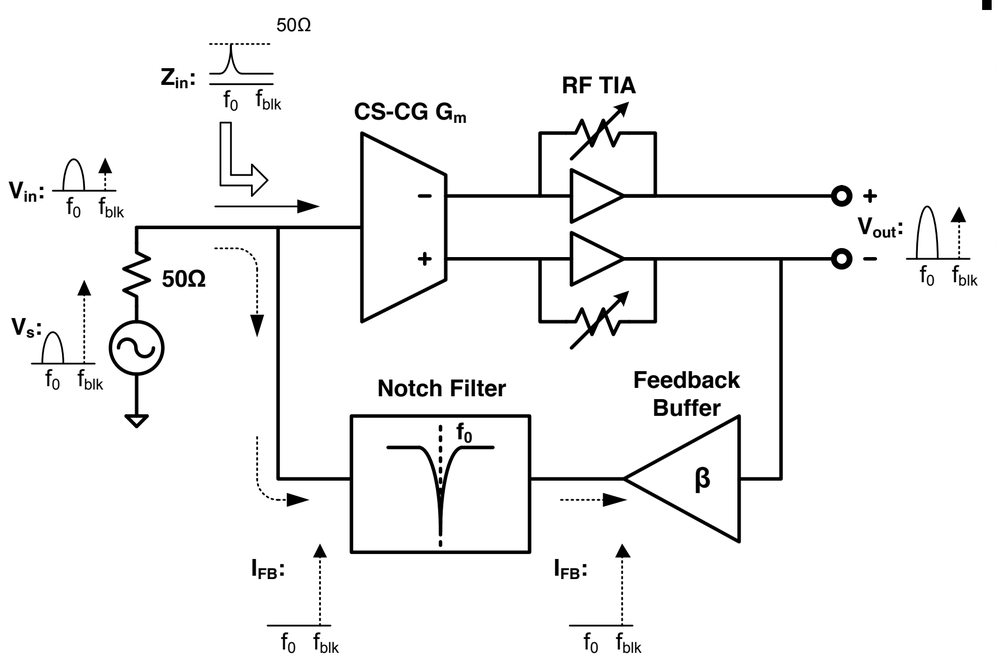
Motivation

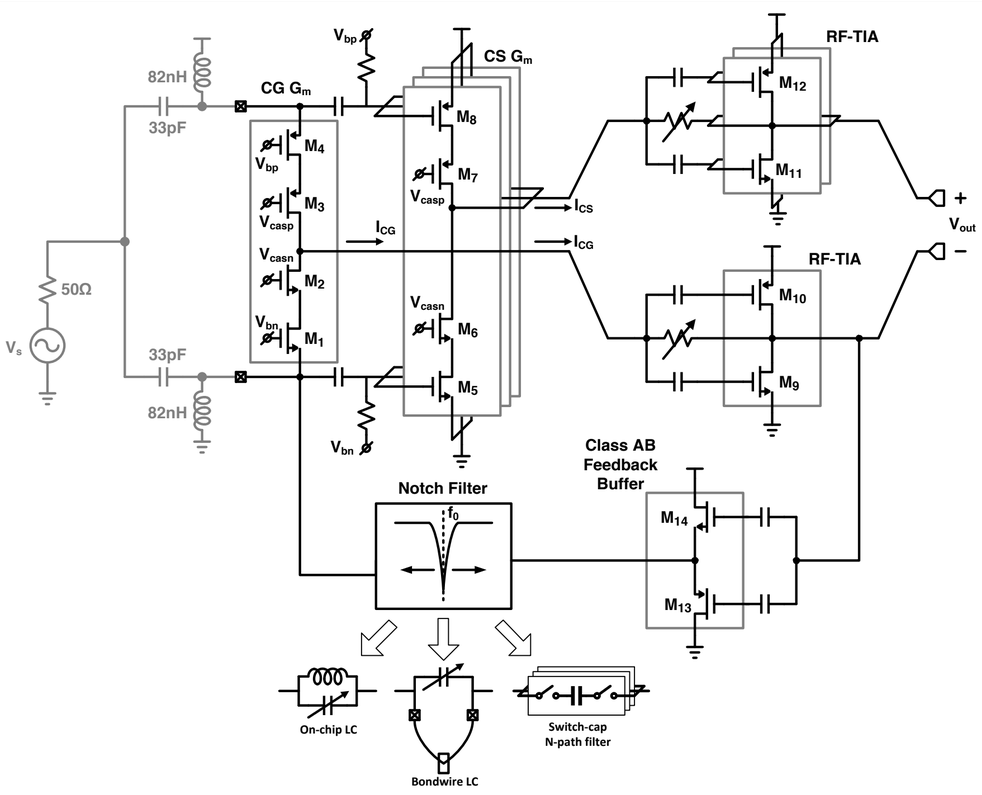
Densely populated RF spectrum imposes stringent linearity requirements on LNA linearity. To accommodate multiple wireless standards, under complex EM environments, LNA specifications such as frequency of operation, Gain, NF and linearity needs to be reconfigured to optimize power consumption. This work explores a highly flexible LNA architecture that is programmable to make power-performance tradeoffs. We also introduce interferer-reflecting techniques that enhances LNA linearity. Two prototype chips are built with passive notch filter tanks and an N-path notch filter driven by 8 phase overlapping clocks.



Principle of Operation of the Interferer-Reflecting Loop

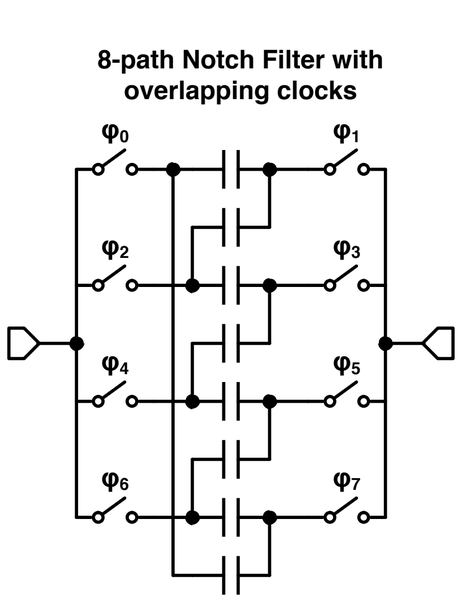
Interferer Reflecting Loop

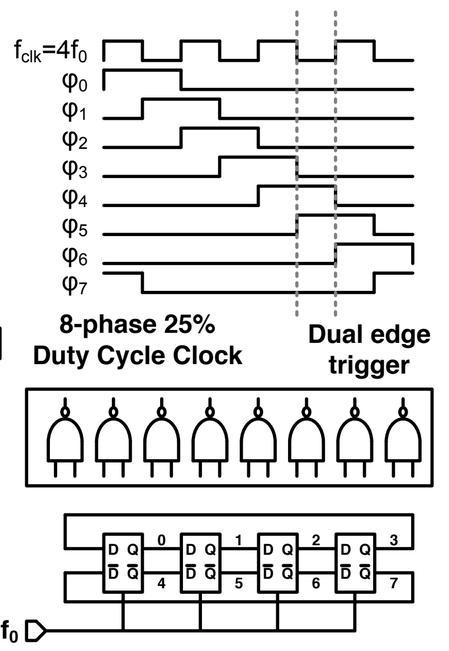
A shunt-shunt feedback loop is built around a wideband noise cancelling LNA. A notch filter is placed in the feedback loop centered at the frequency of interest. At this frequency, the notch filter breaks the feedback loop so that input matching and voltage gain are preserved. Out-of-band blockers, however, see a lower input impedance created by the shunt-shunt feedback. Thus, the voltage swing at the LNA input is reduced . We name this technique interferer reflection as the interferer is rejected with a mismatched input impedance. Noise from the feedback buffer is filtered out by the notch filter when operating in band.



Simplified Schematic

The IR-LNA has a feed-forward path with current reusing noise cancelling G_m amplifiers followed by programmable RF TIAs. The current reusing structure enables the LNA to operation at higher VDD for larger voltage headroom. Each cascode Gm cell can be turned off by switching off the cascode devices. By doing so, NF of the LNA can be traded off with the power consumption. The feedback path consists of a class AB high linearity driver and a tunable notch filter. The notch filter is implemented with three techniques, on-chip LC, on-chip capacitor with bondwire inductors, and switch cap N-path filter.

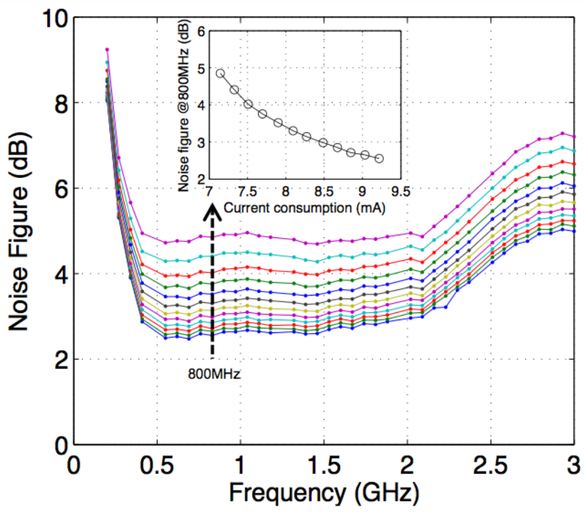




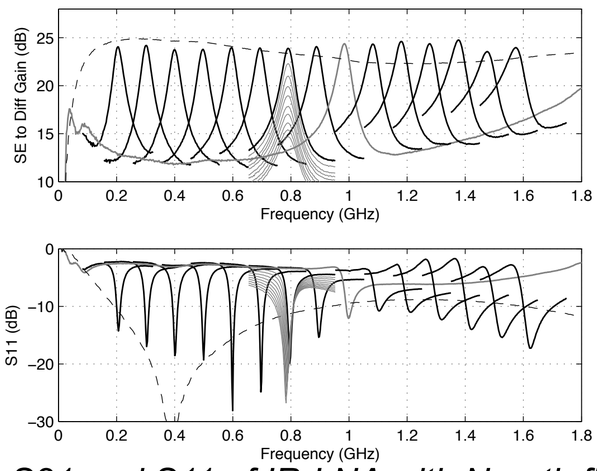
Operation of the N-path Notch Filter

Measurement Results

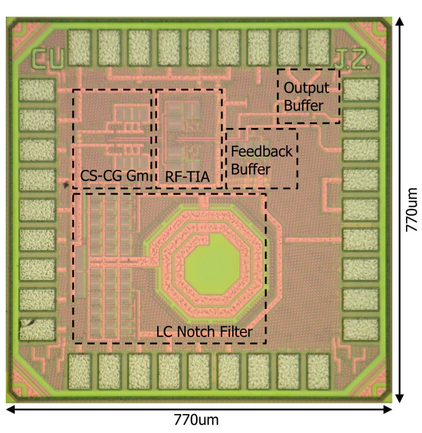
The prototype chips are designed and fabricated with TSMC 65nm technology. The operation frequency can be tuned between 0.2GHz and 1.6GHz with constant 20MHz bandwidth. Voltage gain is programmable from 15dB to 24dB. The minimum noise figure is 2.4dB with IR-loop disabled and 4.2dB with IR-Loop enabled. The LNA draws 8.1mA DC current from the 1.6V analog supply. The IR-loop consumes 1.1mA analog current and 1.1mA to 5.5mA from LO supply. Thanks to the attenuation of the interferer at the LNA input, B1dB-CP is improved by 10dB from -14dBm to -4dBm. Out-of-band IIP3, measured with test tones at 800MHz+foffset and 800MHz+2foffset, improves up to 13.5dB from +1dBm to +14.5dBm.



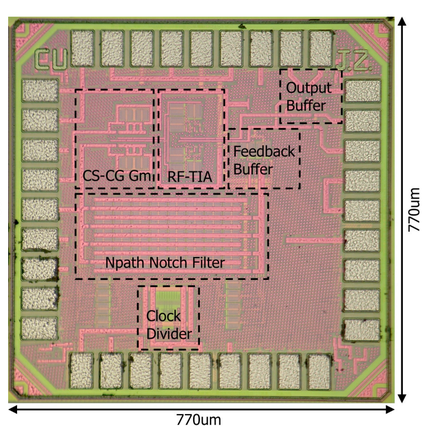
NF – P_{DC} tradeoff using CS G_m Slices



S21 and S11 of IR-LNA with N-path filter



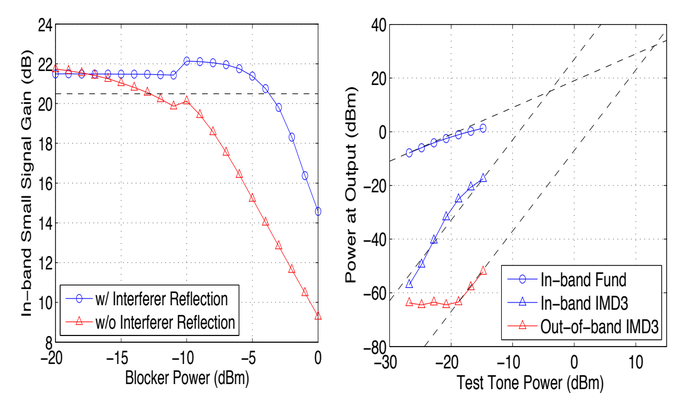
LC filter chip



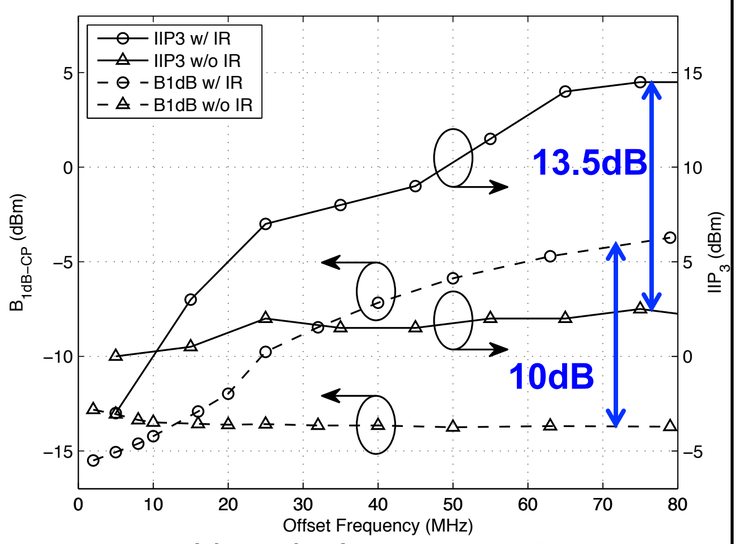
N-path filter chip

Reference	This Work	
CMOS Technology	65nm	
Linearity Enhancement	w/o Interfer Reflection	w/ Interferer Reflection
Frequency (GHz)	0.1-2	0.2-1.6
Gain (dB)	13-22	14-24
NF (dB)	2.4	4.2
OB IIP3 (dBm)	+1	+14.5
B1dB-CP (dBm)	-15	-4
Analog Power Consumption (mA)	8.1	9.2
LO Power Consumption (mA)	0	1.1-5.5
Power Supply (V)	1.6 (Analog) / 1.0 (LO)	

Performance Summary



At 80MHz offset Frequency



Linearity Improvements

Conclusions

The field-programmable interferer-reflecting LNA is a highly flexible architecture that can dynamically program gain, noise figure, linearity and power consumption. The LNA performance can be adjusted for different RF environments with optimal power consumption. The interferer reflecting loop is an effective technique to improve LNA input linearity. Combined with a low-power 8-path notch filter, this IR scheme is highly programmable and offers a very power efficient linearization technique.

Acknowledgments

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