The CMOS common-source amplifier

(a) Diagram of CMOS common-source amplifier with transistors Q1, Q2, and Q3.

(b) Graph showing the relationship between $Q_2$ in triode and saturation regions, with $i = I_{REF}$.

(c) Graph showing the load curve and $v_{GS1} = V_{IB}$ for $Q_1$ in triode and saturation.

(d) Graph showing the voltage $v_O$ with regions I, II, III, and IV, corresponding to $Q_1$, $Q_2$, triode, and saturation, respectively.

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The CMOS common-gate amplifier
The source follower

(a) circuit;
(b) small-signal equivalent circuit
(c) simplified version of the equivalent circuit.
NMOS amplifier with enhancement load

graphical determination of the transfer characteristic

transfer characteristic.
The NMOS amplifier with depletion load: (a) circuit; (b) graphical construction to determine the transfer characteristic; and (c) transfer characteristic.
Small-signal equivalent circuit of the depletion-load amplifier

With the body effect of Q₂.
The CMOS inverter

Simplified circuit schematic for the inverter.
v₁ is high: (a) circuit with v₁ = V_DD (logic-1 level, or V_OH); (b) graphical construction to determine the operating point; and (c) equivalent circuit.
$v_1$ is low: graphical construction to determine the operating point; and (c) equivalent circuit.
Voltage transfer characteristic of the CMOS inverter.

- $V_{OH} = V_{DD}$
- $V_{OL} = 0$
- $V_{th} = \frac{V_{DD}}{2}$
- $Q_N$ in saturation
- $Q_P$ in triode region
- $Q_P$ in saturation
- $Q_N$ in triode region

Slopes:
- $A$ to $B$: $-1$ (for $Q_N$ off)
- $B$ to $C$: $-1$ (for $Q_N$ and $Q_P$ in saturation)
- $C$ to $D$: $-1$ (for $Q_P$ off)
Integrated Circuit Amplifiers
Basic gain cells

Common source

(a)

Common emitter

(b)

Small signal model

(c)

(d)
Intrinsic gain

Technology dependent
Size dependent
Design dependent

\[ g_m = \frac{I_D^{(c)}}{V_{OV}/2} \]
\[ r_o = \frac{V_A}{I_D} = \frac{V_{AV}}{I_D} \]
\[ A_o = \frac{V_A}{V_{OV}/2} \]
\[ A_o \approx 20 - 40 \]

Mutual transconductance
Technology dependent
Temperature dependent

\[ g_m = \frac{I_C}{V_T} \]
\[ r_o = \frac{V_A}{I_C} \]
\[ A_o = g_m r_o = \frac{V_A}{V_T} \]
\[ A_o \approx 200 - 5000 \]
Intrinsic gain

\[ g_m = \frac{I_D^{(c)}}{V_{OV} / 2} \]

\[ r_o = \frac{V_A}{I_D} = \frac{V_A}{I_D} \]

Gain/bandwidth tradeoff
Technology dependent
Size dependent
Design dependent

\[ A_o = \frac{V_A}{V_{OV} / 2} \]
\[ A_o \approx 20 - 40 \]

Mutual transconductance
Technology dependent
Temperature dependent

\[ g_m = \frac{I_C}{V_T} \]

\[ r_o = \frac{V_A}{I_C} \]

\[ A_o = g_m r_o = \frac{V_A}{V_T} \]
\[ A_o \approx 200 - 5000 \]
Alternate view of MOS intrinsic gain

\[ g_m = \frac{I_D}{V_{OV}/2} \]

\[ r_o = \frac{V_A}{I_D} = \frac{V_A'L}{I_D} \]

\[ A_o = \frac{V_A}{V_{OV}/2} \]

\[ g_m = \sqrt{2\mu_n C_ox (W/L)} \sqrt{I_D} \]

\[ A_o = \frac{V_A'}{\sqrt{2\mu_n C_ox (W/L)}} \frac{1}{\sqrt{I_D}} \]
Intrinsic gain of MOSFET

\[ \mu_n C_{ox} = 20 \mu A/V^2 \]

\[ V'_A = \frac{20}{\mu m} \]

\[ L = 2 \mu m \]

\[ W = 20 \mu m \]

Subthreshold region

Strong inversion region

Slope = \(-\frac{1}{2}\)
Intrinsic gain of MOSFET

$A_0$ (log scale)

Subthreshold region

Strong inversion region

BJT-like operation

Extremely low drive current

$\mu_nC_{ox} = 20 \mu A/V^2$

$V_A' = 20 V/\mu m$

$L = 2 \mu m$

$W = 20 \mu m$

Slope $= \frac{-1}{2}$

$A_0 (log scale)$

$I_D$ (A) (log scale)
Increasing gain of basic cell

Standard circuit

Added current buffer to raise output resistance
Increasing gain of basic cell

Standard circuit

Added current buffer to raise output resistance

"Cascode" circuit (cascaded cathode)
Cascode Amplifier

DC bias, Signal ground

$V_{G2}$

$Q_1$

$Q_2$

$r_{o1}$

$K_{r_{o1}}$

To Load

$g_m v_i$

$K_{r_{o1}}$

$V_{i}$

Signal ground

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Cascode Amplifier

Current buffer (common gate)

Basic common source amplifier
Double Cascode

\[ (g_{m3}r_{o3})(g_{m2}r_{o2})r_{o1} = A_0^2 r_o \]

\[ (g_{m2}r_{o2})r_{o1} \]

\[ r_{o1} \]
Folded Cascode

Eliminates limit of power supply voltage
BJT Cascode

Double cascoding of BJTs is not practical due to limitation of maximum output resistance
BiCMOS Cascode

High gain from higher $\beta$ of BJT

Extremely high input impedance

Use of NMOS allows double cascode