CpE358/CS381
Switching Theory and Logical Design
Class 6
Today

- Fundamental concepts of digital systems (Mano Chapter 1)
- Binary codes, number systems, and arithmetic (Ch 1)
- Boolean algebra (Ch 2)
- Simplification of switching equations (Ch 3)
- Digital device characteristics (e.g., TTL, CMOS)/design considerations (Ch 10)
- Combinatoric logical design including LSI implementation (Chapter 4)
- Flip-flops and state memory elements (Ch 5)
- Sequential logic analysis and design (Ch 5)
- Hazards, Races, and time related issues in digital design (Ch 9)
- Synchronous vs. asynchronous design (Ch 9)
- Counters, shift register circuits (Ch 6)
- Memory and Programmable logic (Ch 7)
- Minimization of sequential systems
- Introduction to Finite Automata
Characteristics of Combinatorial Circuits

• Linear signal flow – input to output
• No feedback paths
• No storage elements

![Combinatorial Circuit Diagram](image-url)
Asynchronous Sequential Circuit

\[ \bar{I} \]
\[ n \text{ inputs} \]
\[ \vdots \]
\[ \bar{O} \]
\[ m \text{ outputs} \]

Combinational Circuit

Delay Element(s)
Synchronous Sequential Circuit

\[ \overline{I} \]
\[ n \text{ inputs} \]

\[ \overline{O} \]
\[ m \text{ outputs} \]

Clock

Combinational Circuit

Storage Element(s)
Feedback Paths in Logic Circuits

• Condition of signal leads is indeterminate
Feedback Paths in Logic Circuits

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Feedback Paths in Logic Circuits

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Feedback Paths in Logic Circuits

- Condition of signal leads is indeterminate
Feedback Paths in Logic Circuits

• Condition of signal leads is indeterminate

• With some technologies (e.g., CMOS) this can actually be used to build an oscillator \( f \sim 1/(3t_d) \)
Basic Storage Element - Latches

• NOR gate “S-R” Latch

![Diagram of NOR gate S-R Latch]

<table>
<thead>
<tr>
<th>S</th>
<th>R</th>
<th>Q</th>
<th>Q'</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

Values Held

![Timing diagram for S-R Latch]
Basic Storage Element - Latches

- NAND gate “S-R” Latch

\[
\begin{array}{c}
\text{S} \\
\text{R} \\
\text{Q} \\
\text{Q'}
\end{array}
\quad
\begin{array}{c}
1111 \\
0111 \\
0110 \\
1011 \\
1001 \\
\end{array}
\]

\[
\begin{array}{c|c|c|c}
S & R & Q & Q' \\
1 & 0 & 0 & 1 \\
1 & 1 & 0 & \text{red circle} \\
0 & 1 & 1 & 0 \\
1 & 1 & 1 & \text{red circle} \\
1 & 1 & 1 & 1 \\
\end{array}
\]

Values Held

\[
\begin{array}{c}
\text{S} \\
\text{R} \\
\text{Q} \\
\text{Q'}
\end{array}
\quad
\begin{array}{c}
\text{S} \\
\text{R} \\
\text{Q} \\
\text{Q'}
\end{array}
\]

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Basic Storage Element - Latches

- NAND gate “S-R” Latch with control input

<table>
<thead>
<tr>
<th>C</th>
<th>S</th>
<th>R</th>
<th>Q_{i+1}</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>X</td>
<td>X</td>
<td>Q_i</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>Q_i</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>?</td>
</tr>
</tbody>
</table>

Diagram of the NAND gate “S-R” Latch with control input.
Basic Storage Element - Latches

- D Latch with control input

```
+---+---+---+
| C | D | Q |
+---+---+---+
| 0 | X | Q_i |
+---+---+---+
| 1 | 0 | 0  |
+---+---+---+
| 1 | 1 | 1  |
```
Limitations of Level Sensitive Latches

• What is timing of D vs. C?

D
C
Q

• A slight change in timing could produce different results:

D
C
Q
Master-Slave D Flip-Flop

\[ Q(t + 1) = D \]
Master-Slave Timing

Master doesn’t change while $C'$ high

Slave Q guaranteed stable
Variations of D Flop-flops

Positive Edge Triggered

Negative Edge Triggered
J-K Flip Flop

\[ Q(t + 1) = JQ' + K'Q \]

<table>
<thead>
<tr>
<th>J</th>
<th>K</th>
<th>( Q_{i+1} )</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>( Q_i )</td>
<td>No change</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>Clockin 1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>Clockin 0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>( Q_i' )</td>
<td>Toggle</td>
</tr>
</tbody>
</table>

Constructing a J-K from a D

Constructing a D from a J-K
Toggle Flip Flop

\[ Q(t+1) = T \oplus Q \]

Constructing a T from a JK

Constructing a T from a D

<table>
<thead>
<tr>
<th>T</th>
<th>Qi+1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Qi</td>
<td>No change</td>
</tr>
<tr>
<td>1</td>
<td>Qi'</td>
<td>Toggle</td>
</tr>
</tbody>
</table>
Immediate Inputs to Flip-Flops

- Sometimes referred to as Preset and Clear, the immediate inputs can be used to preset a known state at startup.

<table>
<thead>
<tr>
<th>J</th>
<th>K</th>
<th>S</th>
<th>R</th>
<th>Q_{i+1}</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>Q_{i}</td>
<td>No change</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>Clockin 1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>Clockin 0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>Q_{i}</td>
<td>Toggle</td>
</tr>
<tr>
<td>X</td>
<td>X</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>Set</td>
</tr>
<tr>
<td>X</td>
<td>X</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>Reset</td>
</tr>
<tr>
<td>X</td>
<td>X</td>
<td>0</td>
<td>0</td>
<td>?</td>
<td>Undefined</td>
</tr>
</tbody>
</table>
Generic Sequential Clocked Sequential Circuit

\[ \bar{i} \rightarrow \text{Combinational Circuit} \rightarrow \bar{O} \]

\[ n \text{ inputs} \rightarrow \text{Combinational Circuit} \rightarrow m \text{ outputs} \]

Clock

\[ \text{Storage Element(s)} \]
Generic Sequential Clocked Sequential Circuit

Storage elements contain system state

Combinational circuit determines next state

\[ \bar{i} \]
\[ n \text{ inputs} \]

\[ \text{Combinational Circuit} \]

\[ \bar{o} \]
\[ m \text{ outputs} \]

\[ \text{System State} \]

\[ \text{Next State} \]

\[ \text{Storage Element(s)} \]
Abstraction of Sequential Circuit

[Diagram showing the flow between inputs, state, state transition, and outputs]
Abstraction of Sequential Circuit

- State
- Outputs

- Boolean Equations
- Truth Table
- Karnaugh Map
- Logic Diagram

- State Transition Controls

- Inputs
Abstraction of Sequential Circuit

Boolean Equations
Truth Table
Karnaugh Map
Logic Diagram

Inputs

State Transition Controls

State equations
State table
State diagram
Typical Sequential Circuit With No Inputs
Typical Sequential Circuit With No Inputs

- Description by State Equations

\[ A(t+1) = B(t) \oplus C(t) \]
\[ B(t+1) = A(t) \]
\[ C(t+1) = B(t) \]

\[ A(t+1) = B(t+1) = A(t) \]
\[ C(t+1) = B(t) \]
Typical Sequential Circuit With No Inputs

• Description by State Table

<table>
<thead>
<tr>
<th>Present State</th>
<th>Input</th>
<th>Next State</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>A  B  C</td>
<td>-</td>
<td>A  B  C</td>
<td>-</td>
</tr>
<tr>
<td>0  0  0</td>
<td>-</td>
<td>0  0  0</td>
<td>-</td>
</tr>
<tr>
<td>0  0  1</td>
<td>-</td>
<td>1  0  0</td>
<td>-</td>
</tr>
<tr>
<td>0  1  0</td>
<td>-</td>
<td>1  0  1</td>
<td>-</td>
</tr>
<tr>
<td>0  1  1</td>
<td>-</td>
<td>0  0  1</td>
<td>-</td>
</tr>
<tr>
<td>1  0  0</td>
<td>-</td>
<td>0  1  0</td>
<td>-</td>
</tr>
<tr>
<td>1  0  1</td>
<td>-</td>
<td>1  1  0</td>
<td>-</td>
</tr>
<tr>
<td>1  1  0</td>
<td>-</td>
<td>1  1  1</td>
<td>-</td>
</tr>
<tr>
<td>1  1  1</td>
<td>-</td>
<td>0  1  1</td>
<td>-</td>
</tr>
</tbody>
</table>
Typical Sequential Circuit With No Inputs

- Description by State Diagram
Mealy/Moore Models

• Output is a function of state only = Moore Model

![Diagram of Mealy/Moore Models]

- State
- State Transition Controls
- Outputs
- Inputs
Mealy/Moore Models

• Output is a function of state and inputs = Mealy Model
Summary

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Homework 6 – due in Class 8

• As always, show all work
• Problems 5-6, 5-8, 5-9